AN_6511_023

APPLICATION NOTE

SEPTEMBER 2005

EMI/EMC Compliant Meter Design

A meter design based on a 2-layer PCB that passes EMI/EMC tests, such as radiated and conducted emissions, radiated susceptibility, as well as EFT is presented in this application note. Design techniques used to achieve the desired results are explained.

Introduction

Designing a meter for optimum electromagnetic compatibility can be a challenging issue for any design engineer. EMC/EMI testing for metering products involve the Conduced and Radiated Emissions, RF Immunity, Electro-static Discharge (ESD) and Electrical Fast transient (EFT) testing. Successfully passing these tests depends on many factors, such as schematic design, PCB layout, component selection, component placement on the PCB and the input connections of the current sensing elements to the meter. The methods presented in this document provide EMI suppression without affecting accuracy performance of the meter.

Following the recommendations outlined in this document in the initial phase of schematic and PCB design helps generating EMI/EMC compliant designs up front, avoiding potential rework of PCBs.

This document describes the details for EMI/EMC compliance based on a 2-layer 71M6511 Demonstration Board.

Schematic Design Precautions

In this section, details of schematic design for critical areas of the meter will be discussed.

Current Inputs:

Figure 1 shows the suggested input signal conditioning circuit for Current Shunt inputs.

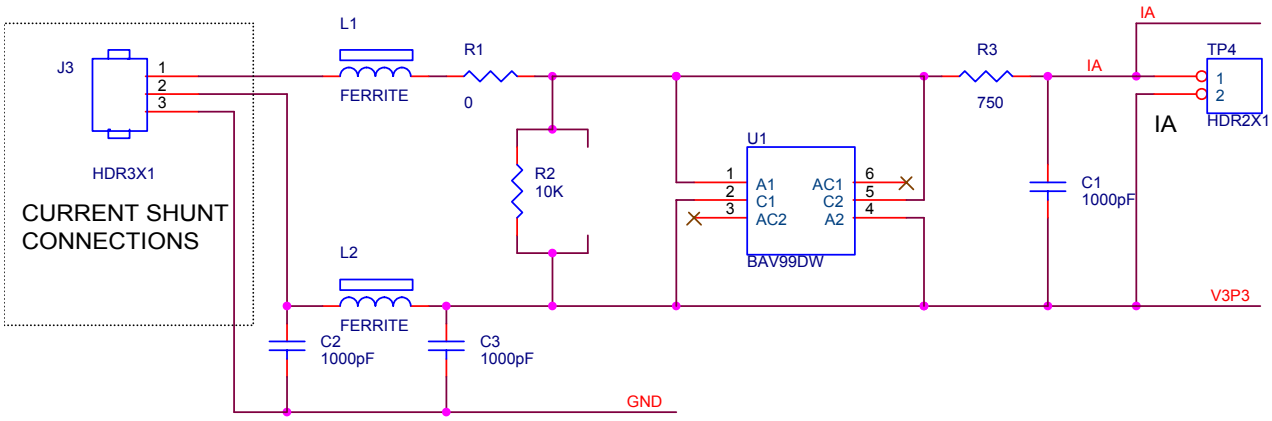
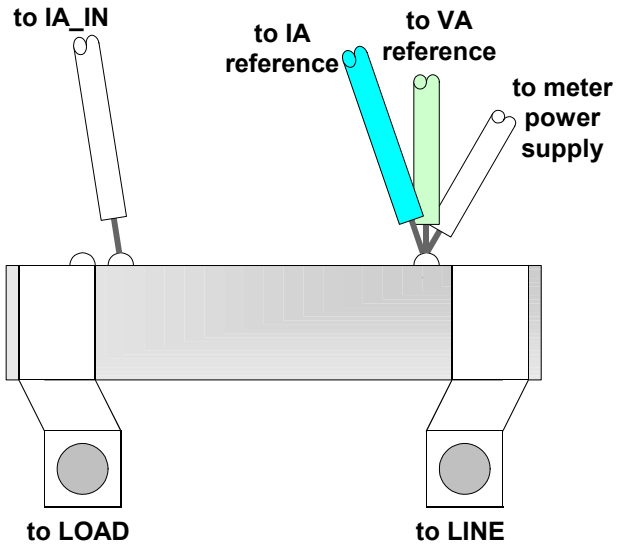


Figure 1: Current Shunt Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. Generally, the Current Shunt interface to 71M6511 Demo Boards involves a four-wire connection, as shown below. Two of the wires connect as shunt inputs for the current sensing circuit and the other two wires are tied to one side of the shunt along with one of the current sensing wires. These two wires may also need to be shielded and the shield should then be connected to digital ground of the PCB.



2. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
3. R3 and C1 provide a low pass filter for differential signals. Depending on the length of the cable harness used to hook up the current shunt, the value of the capacitor C1 may vary.
4. Connector J3 has a third pin provision to accommodate for the connection to the shield of the Shunt cable to connect to the digital ground to prevent high frequency noise entering through the Shunt metal plate and the connecting cables.
5. C2, L2 and C3 form a Pi-filter that eliminates high-frequency noise spikes on the analog reference, V3P3.
6. R2 is in parallel to the Shunt Resistor and will increase the signal-to-noise ratio.
7. R1 is 0Ω.

Note: Using a shunt resistor involves proper wiring, both on the circuit board and outside towards the shunt resistor. The importance of proper wiring will be explained using Figure 2. In Figure 2, only one wire is used to connect V3P3 to the NEUTRAL terminal at the shunt resistor. Consequently:

- During operation, the meter will draw its entire power through this wire (current 1)
- Node A (V3P3) functions as a reference for the measured voltages.
- Part of current 1 is used for the power supply (current 2) and to power the IC (current 3)
- Current 4 flows through the resistor divider, establishing the voltage at VA.

Because of the varying current powering the meter the voltage at node A is modulated by a few µV with respect to IA and VA. Since the ADC in the 71M6511 measures the analog input signals referenced to V3P3, the modulation will find its way into the sampled values.

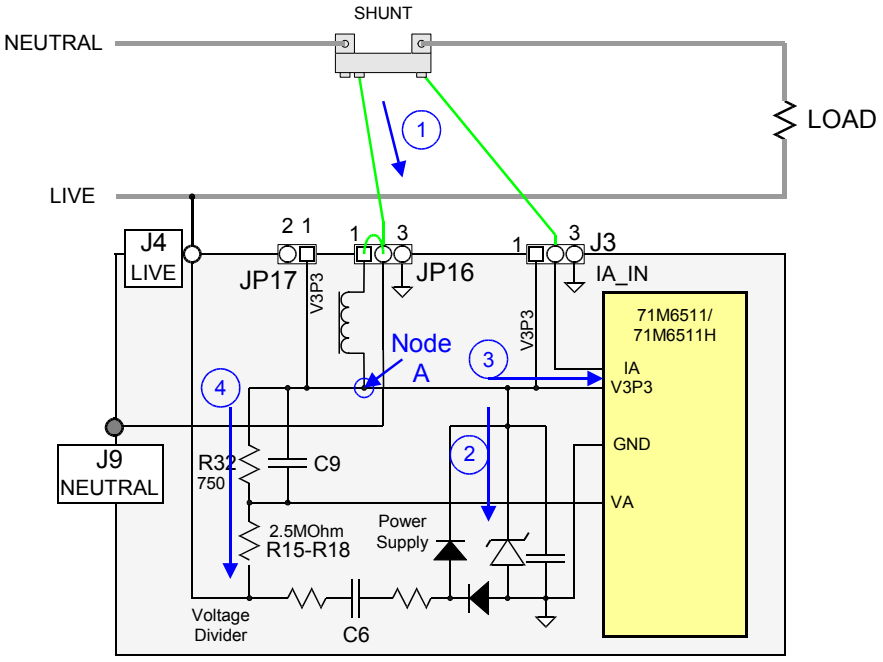


Figure 2: Wrong Current Shunt Wiring

The solution is to separate the wire carrying the modulated supply current from the sensitive references. If we open up the junction at node A, and route the V3P3 net from the 71M6511 as well as the line going to R2 separately to the shunt resistor (as shown in Figure 3), we have successfully separated the sensitive connections from the modulated connections.
Using the connection shown in Figure 3, the supply current modulation only influences the V3P3-to-ground voltage, where a few µV will cause no harmful effects due to the good power supply rejection ratio of the 71M6511.

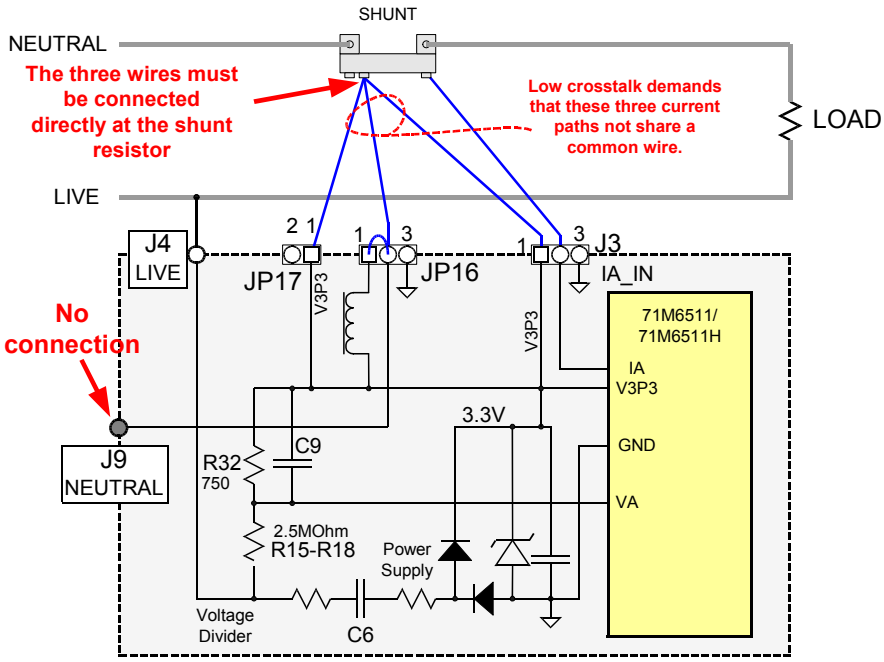


Figure 3: Improved Current Shunt Wiring

Voltage Inputs

Figure 4 shows the circuit to be used when a 6511 Board is operated in current shunt mode. When using the Demo Boards, JP17 is left open and one of the three wires coming from the line side of the current shunt will connect to JP17, pin 2. C3 and L2 have been added for noise protection of this signal. Capacitor C2 in Figure 4 appears as C14 on the Demo Boards.

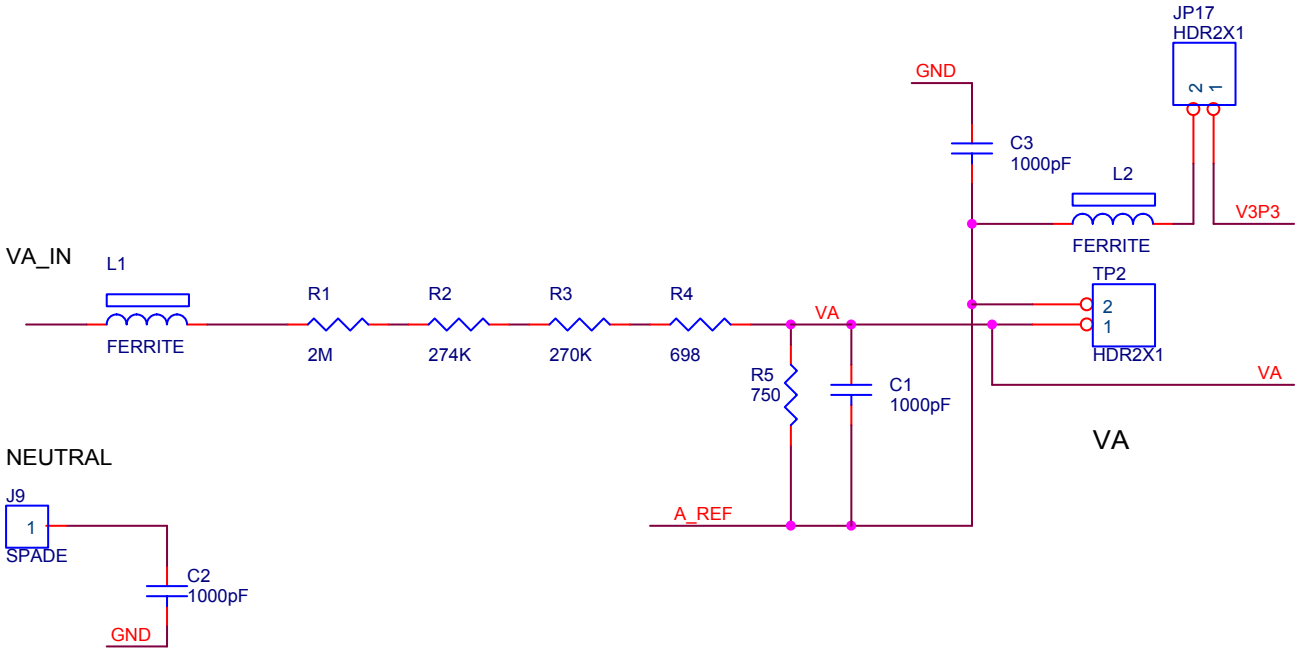


Figure 4: Voltage Input Circuit for Current Shunt Mode

Power Supply Circuit

Figure 5 shows the suggested power supply circuit (power supply with capacitive coupling). In general, power supplies using transformers will provide better results in EMC/EMI testing.

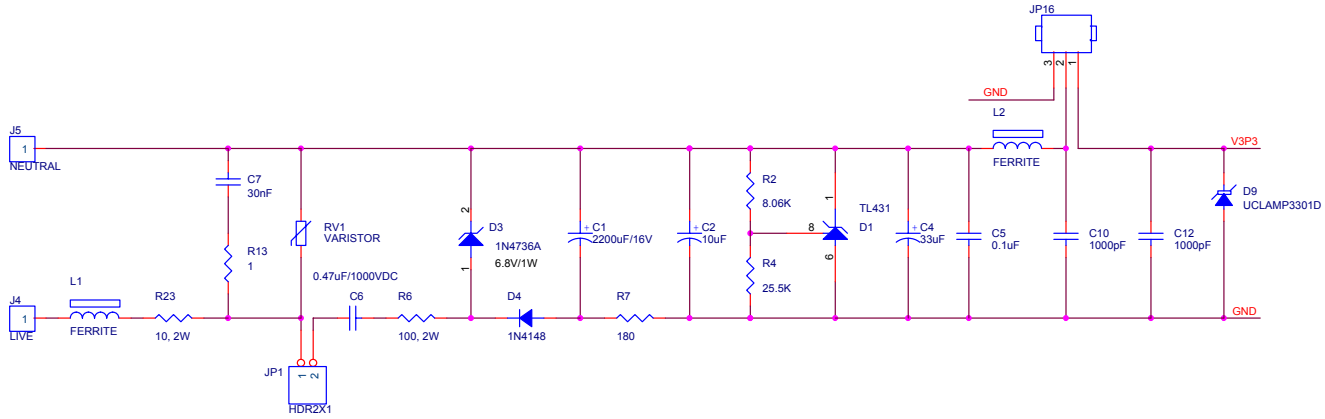


Figure 5: Power Supply Circuit

Key precautions recommended for the power supply circuit are:

1. The Ferrite bead L2 at the V3P3 output prevents high frequency noise.
2. A TVS (Transient Voltage Suppressor D9) is added to clamp the V3P3 supply voltage to 3.3V. This device may be a bi-directional clamping device to prevent high voltage peaks into the circuit, e.g. the SEMTECH UCLAMP3301D.
3. The resistor R23 is added in series to the varistor (MOV) to limit the surge current. This resistor will cause a voltage drop that helps protecting both the varistor and the meter circuitry. The resistor may be a flame-proof 10Ω type rated 3W to 5W.
4. The high-voltage capacitor C7 is added in parallel to the varistor to suppress high-frequency noise. The series resistor R13 (1Ω) is used to dampen oscillations that may occur due to the effective impedance of the power supply.
5. C10 and C12 suppress high-frequency noise.

Reset Circuit

Noise spikes on the V3P3 net can enter the IC through the RESETZ pin and cause unwanted hardware resets. This situation can be eliminated by applying proper filtering, as shown in Figure 6. Long traces leading to the RESETZ pin must be avoided.

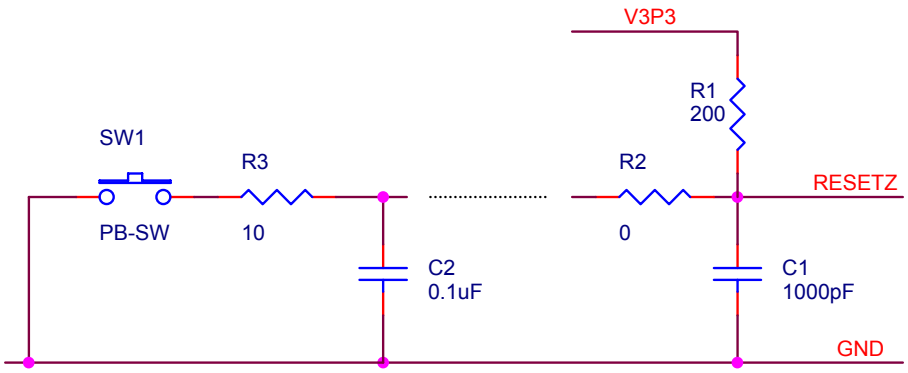


Figure 6: Reset Circuit

It is beneficial to terminate the RESETZ signal very close to the 651X chip with a strong pull-up resistor and a small capacitor (R1 and C1 in Figure 6). If the reset pushbutton cannot be located right at the chip, another resistor (R2) should be provided between the RESETZ net and the switch. Removing this resistor will separate the switch from the RESETZ pin to ensure proper function in severe EMI/EMC environments.

V1 Circuit

V1 is the power fault input to the 651X IC. It tends to pick up noise when not properly terminated. Any disturbance reaching this pin (e.g. from sensors connected to V3P3) can potentially drive the IC into reset. Long traces leading to the V1 pin must be avoided.

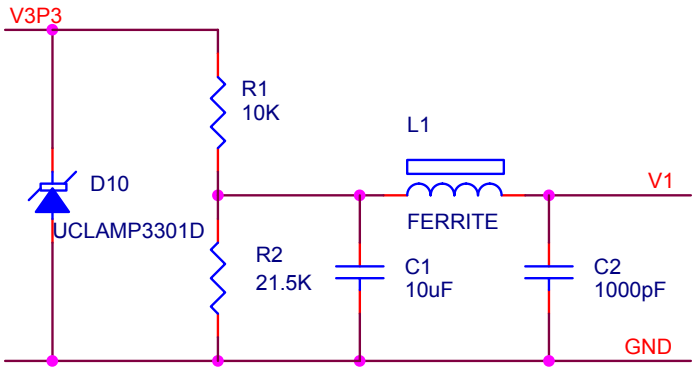


Figure 7: V1 Circuit

V1 should be decoupled with a 10µF tantalum capacitor to ground and held close to 2.5VDC, e.g. by a voltage divider of 6.81kΩ/21.5kΩ. The capacitor C2 (in Figure 7), in conjunction with the ferrite L1, helps eliminating high-frequency noise.
Adjusting V1 too low can have the effect that short sags of the V1 voltage could drive the IC into reset.
Adjusting V1 too high can cause the hardware watch dog timer to be disabled which is not desirable.

Other 651X IC Signal Pins

All signals from and to the 651X IC have to be carefully examined for EMI susceptibility. Careful termination helps to defeat unwanted resets or false readings caused by RF fields.

Following are the precautions for the other IC pins on the demo board/ 71M651X:

1. Signal input pins (**IA, IB, IC, VA, VB, VC**): All unused current and voltage inputs should be tied to V3P3.
2. A 10µF tantalum capacitor should be used between the **V3P3A** pin of the IC and ground. It should be mounted as close as possible to the 651X IC (C18 on the Demo board)
3. The **VREF** pin should be bypassed with a 0.1µF capacitor to ground and another 0.1µF capacitor to V3P3.
4. Any unused signal nets should be cut and terminated as closely to the IC as possible. For the Demo Board this means that the switch SW1, R100 through R102, R112 through R116, and all connections to the debug connector should be removed.
5. A 0.1µF capacitor should be placed between the **V2P5** pin and ground. This improves the operation of the internal regulator used to generate 2.5VDC from 3.3VDC by reducing ripple.
6. Strong pull-up resistors (1kΩ) should be used for the emulator signals (**E_RST, E_TCLK, E_TXRX**) in order to support the relatively weak internal pull-up resistors in the IC.
7. Pins **OPT_TX** and *OPT_RX*, when not used, should be tied to V3P3.
8. Unused SSI/segment pins should be disabled on the Demo Boards by removing the resistors R112-R116.
9. When no battery is used, the **VBAT** pin should be tied to V3P3.
10. Unused **DIO** pins should be connected to GND via 10kΩ resistors and should be configured as outputs in the firmware.

Layout Precautions

1. The most successful layouts use four layers, with the two internal layers being ground and V3P3.
2. If two-layer boards are used, the layout has to be designed very carefully:
   - It is helpful to keep the high-voltage and low-voltage sections of the board clearly separated.
   - Ground and V3P3 traces should be widened (using copper pour techniques) to become virtual planes. Naturally, it is impossible to route a 2-layer board with continuous copper planes. However, ground and V3P3 structures can be placed on both sides of the board and then “stitched” together with free vias, creating good connectivity for both V3P3 and ground.
   - For a good example of a two-layer board, examine the 6511 2-Layer Demo Board (see Figure 8 and Figure 9).
3. The V3P3A plane for measurement should be wide enough to act as a stable reference for the measurement signals. The wider the V3P3A copper structure is, the better the measurement performance of the meter will be. All V3P3 structures should come together at a star point close to the V3P3A pin of the IC (see Figure 9).
4. The crystal should be positioned as close as possible to the 71M651x IC and rotated properly to make the traces short. No other traces should cross the traces between the IC and the crystal on the other side of the board. The parallel resistor implemented in some Demo Boards is not needed.
5. Slots cut into the PCB should be used for isolation where high-voltage signals are located close to low-voltage signals. This prevents arching or leakage currents when the PCB surface is not perfectly clean.
6. When laying out the V3P3 traces, a “Kelvin” junction scheme should be used, i.e. all connections should meet at a star point close to the V3P3 pin of the IC.

Firmware/Configuration Precautions

1. All unused DIO pins should be configured as outputs. This way no unwanted signals enter the IC.
2. The emulator clock should be disabled (by configuring *ECK_DIS* to 1) so that no 5MHz clock (I/O RAM 0x2005 Register Bit 5) is generated at the emulator port. This prevents any emissions due to the 5MHz clock signal. This also ensures that the emulator port is disabled.
3. The RTM clock output should be disabled (by configuring *CKOUT_DIS* to 1) when no Real-Time monitoring is performed with the production version of the firmware.
4. Dummy interrupt service routines containing a RETI instruction should be placed at all locations pointed to by unused interrupt vectors.
5. All interrupt service routines (ISRs) should be as short as possible and should be minimized for memory manipulation operations.

71M6511 Reference Design

The design described in this section was submitted to extensive EMI/EMC testing in September 2005. Even though not all recommendations from the previous section were implemented, the meter passed all tests, including the EFT test.

Bill of Material

Table 1 and Table 2 show the components used for the design.

Item	Q	Reference	Part	Footprint	Digi-Key/Mouser P/N	Manuf. P/N	Manufacturer
1	1	C1	2200UF, 16V	radial	P5143-ND	ECA-1CM222	Panasonic
2	2	C2,C34	10UF, 10V	1812	478-1672-1-ND	TAJB106K010R	AVX
3	1	C4	33UF, 10V	1812	478-1687-1-ND	TAJB336K010R	AVX
4	10	C5,C17,C19,C20,C22,	0.1UF	0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C28,C30,C31,C33,C35					
5	1	C6	0.47UF, 1000VDC	block	BC1918-ND	222 383 30474	BC Components
6	12	C8,C10,C14-C16,C18,C23	1000pF	0603	445-1298-1-ND	C1608X7R2A102K	TDK/X7R
		C29,C36-C39					
7	1	C9	220pF	0603	445-1306-1-ND	C1608X7R1H221K	TDK/X7R
8	5	C7,R88,R89,R91,R119	NC	0603	N/A	N/A	N/A
9	2	C24,C25	10pF	0603	445-1269-1-ND	C1608C0G1H100D	TDK/COG
10	1	C26	0.2uF	0603	445-1318-1-ND	C1608X7R1C224K	TDK/X7R
11	1	C27	0.03uF	0603	PCC2284CT-ND	ECJ-1VB1H333K	Panasonic
12	1	C32	0.03uF, 250VDC	AXIAL	75-125LS30	125LS30	Vishay
13	1	C36	0.01uF, 250VDC	AXIAL	75-125LS10	125LS10	Vishay
14	1	D1	TL431	SO8	296-1288-1-ND	TL431AIDR	TI
15	1	D3	1N4736A	DO41	1N4736ADICT-ND	1N4736A-T	DIODES
16	1	D4	1N4148	DO35	1N4148DICT-ND	1N4148-T	DIODES
17	2	D5,D6	LED	LED6513	67-1612-ND	SSL-LX5093SRC/E	LUMEX
18	1	D7	BAT54S/SOT	SOT-23	BAT54SDICT-ND	BAT54S-7	DIODES
19	2	D8,D9	uCLAMP3301D	SOD-323	N/A	UCLAMP3301D.TCT	SEMTECH
20	16	JP1,JP8,JP10,JP17,J13,	HDR2X1	HDR2X1	S1011-36-ND	PZC36SAAN	Sullins
		J3,JP16,J16,TP1,TP2,TP7,					
		TP10,TP17,TP19,TP21-TP22					
21	3	JP2,JP3,JP18	NC	N/A	N/A	N/A	N/A
22	1	J1	DC Connector	DC CONN	SC1152-ND	RAPC712	Switchcraft
23	1	J2	HEADER 8X2	HDR8X2	S2011-36-ND	PZC36DAAN	Sullins
24	1	J4,J9	spade terminal	SPADE	A24747CT-ND	62395-1	AMP
25	2	J12,J16Z	HDR5X1	HDR5X1	S1011-36-ND	PZC36SAAN	Sullins
26	1	J14	0.05" HDR 10X2	HDR0.05	A3210-ND	104068-1	AMP
27	9	L1-L8,L10	Ferrite, 600Ohm	1206	N/A	MMZ2012S601A	TDK
28	1	RV1	VARISTOR	radial	581-VZD510XX	VE24M00511K	AVX
29	1	R2	8.06KK	0603	P8.06KHCT-ND	ERJ-3EKF8061V	Panasonic
30	1	R4	25.5K	0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
31	1	R6	100, 2W	axial	100W-2-ND	RSF200JB-100R	Yageo
32	1	R7	130	1206	311-130FCT-ND	9C12063A1800FKHFT	Yageo
33	1	R8	1	1206	311-1.00FCT-ND	9C12063A1.00FGHFT	Yageo
34	1	R9	68	1206	311-68.0FCT-ND	9C12063A1100FKHFT	Yageo
35	6	R10-R12,R97-R99,	62	0603	311-62.0HCT-ND	9C06031A62R0FKHFT	YAGEO
36	1	R12	0	0603	P0.0GCT-ND	ERJ-3GEYJ00V	Panasonic
37	3	R14,R32,R104	750	0603	P750HCT-ND	ERJ-3EKF7500V	Panasonic
38	1	R15	2M	axial	71-RN65D-F-2.0M		Dale
39	1	R16	274k	805	P274KCCT-ND	ERJ-6ENF2743V	Panasonic

Table 1: 6511 2-Layer Demo Board BOM (1/2)

40	1	R17	270k	805	1-270KCCT-ND	9C08052A2703FKHFT	YAGEO
41	1	R18	698	805	P698CCT-ND	ERJ-6ENF6980V	Panasonic
42	2	R106,R107	3.4	1206	311-3.40FCT-ND	9C12063A3R40FGHFT	Yageo
43	6	R13,R24,R74,R76,R83,R94	10K	0603	P10.0KHCT-ND	ERJ-3EKF1002V	Panasonic
44	1	R77	10	0603	P10.0HCT-ND	ERJ-3EKF10R0V	Panasonic
45	1	R79	100	0603	P100HCT-ND	ERJ-3EKF1000V	Panasonic
46	4	R82,R88,R89,R119	1K	0603	P1.00KHCT-ND	ERJ-3EKF1001V	Panasonic
47	2	R108,R109	3K	0603	P3.00KHCT-ND	ERJ-3EKF3001V	Panasonic
48	1	R84	47K	0603	311-47.0KHCT-ND	9C06031A4702FKHFT	YAGEO
49	1	R86	21.5K	0603	P21.5KHCT-ND	ERJ-3EKF2152V	Panasonic
50	2	R110,R111	0	1206	P0.0ECT-ND	ERJ-8GEY0R00V	Panasonic
51	1	R118	10, 2W	axial	10W-2-ND	RSF200JB-10R	Yageo
52	1	SW2	PB SWITCH	PB	P8051SCT-ND	EVQ-PJX05M	Panasonic
53	3	TP13,TP14,TP15	TESTPOINT	TESTPOINT	5011K-ND	5011	Keystone
54	1	TP20	HEADER 5X2	HDR5X2	S2011-36-ND	PZC36DAAN	Sullins
55	2	U1,U6	BAV99DW	SOT-363	BAV99DWDICT-ND	BAV99DW-7	DIODES
56	1	U4	SER EEPROM	SOIC8	AT24C1024W10SI2.7-ND	AT24C1024W-10SI-2.7	ATMEL
57	1	at U5	64TQFP SOCKET	64TQFP	N/A	64TQFP SOCKET	YAMAICHI
58	1	U5	71M6511H-IGT	64TQFP	N/A	71M6511H-IGT	TDK
59	1	U7	VIM-808-DP	LCD	153-1056-ND	VIM-808-DP-RC-S-HV	Varitronix
60	1	Y1	32.768KHZ	XTAL	XC488CT-ND	ECS-.327-12.5-17-TR	ECS

Table 2: 6511 2-Layer Demo Board BOM (2/2)

Layout

Figure 8 and Figure 9 show the top and bottom level copper of the PCB.

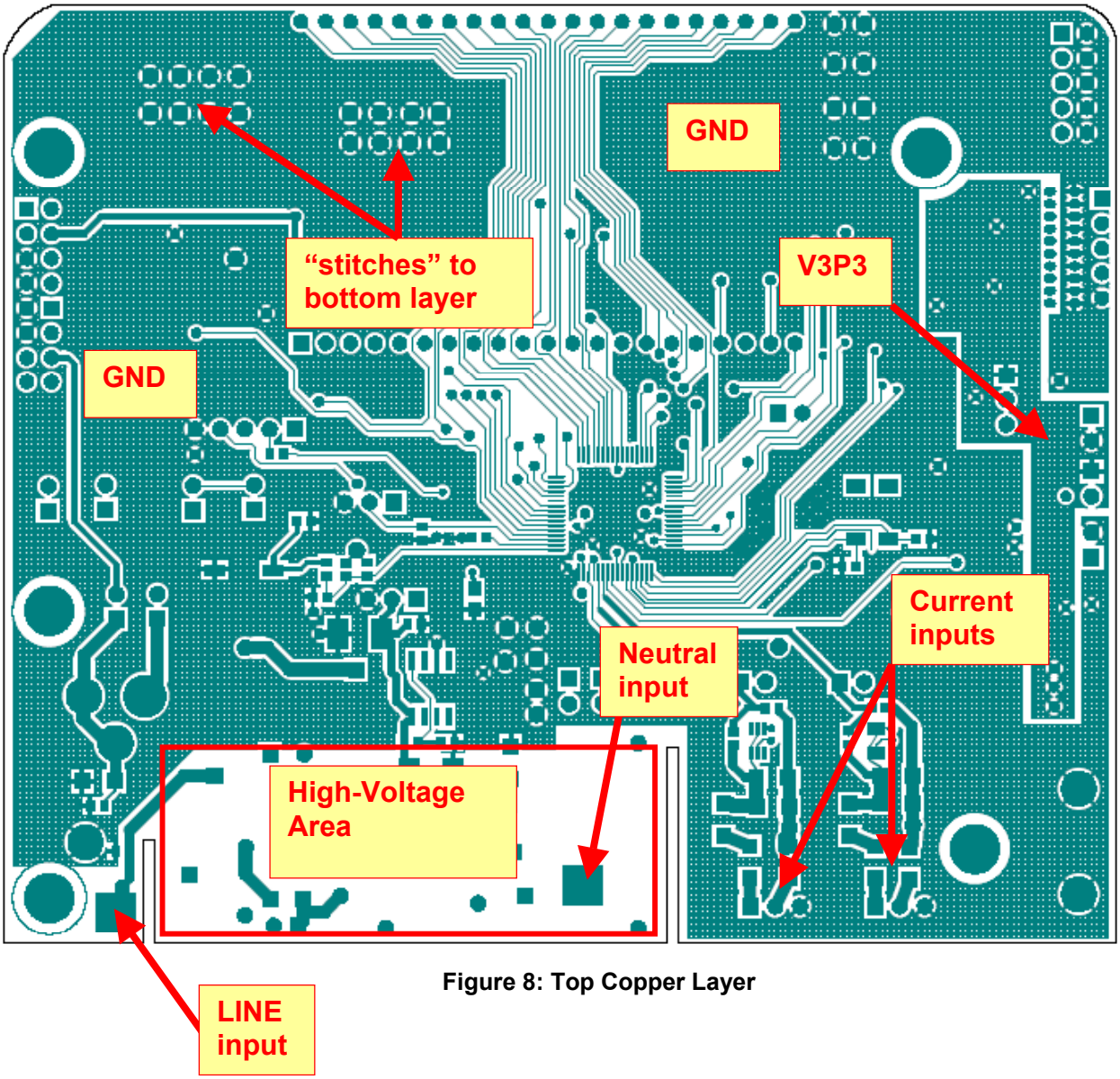


Figure 8: Top Copper Layer

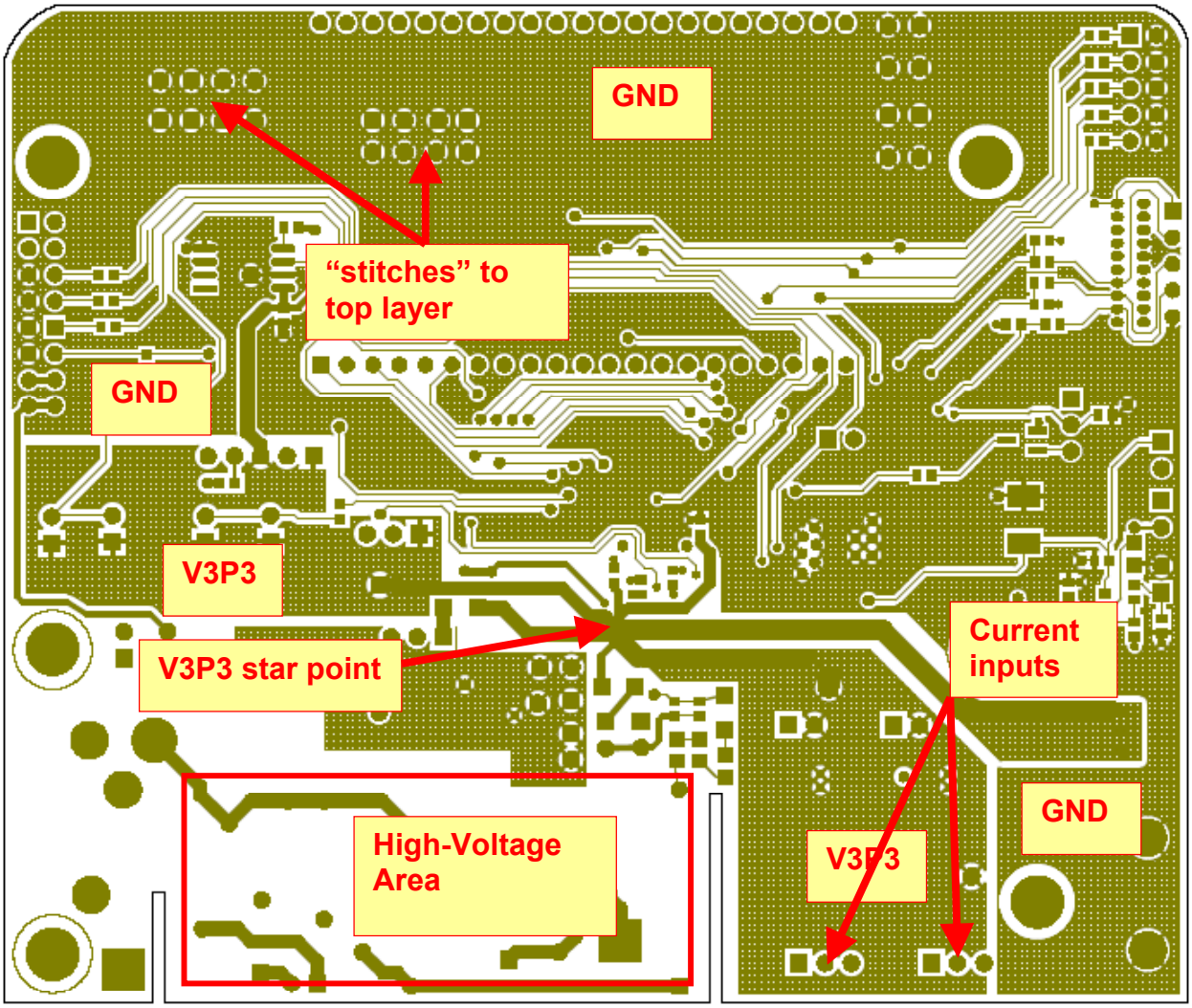


Figure 9: Bottom Copper Layer

Schematics

Figure 10, Figure 11, and Figure 12 show the schematic design.
The IA input functions as the input for the shunt resistor signal. R24/R25 from the original configuration have been removed, and a 10kΩ resistor has been installed to eliminate noise. The IB input (see Figure 11) has been left unchanged, since it is not used (a jumper across TP19 disables the input to the 71M6511 IC). The IB input may be used for a CT in combined CT/shunt configurations, if needed.

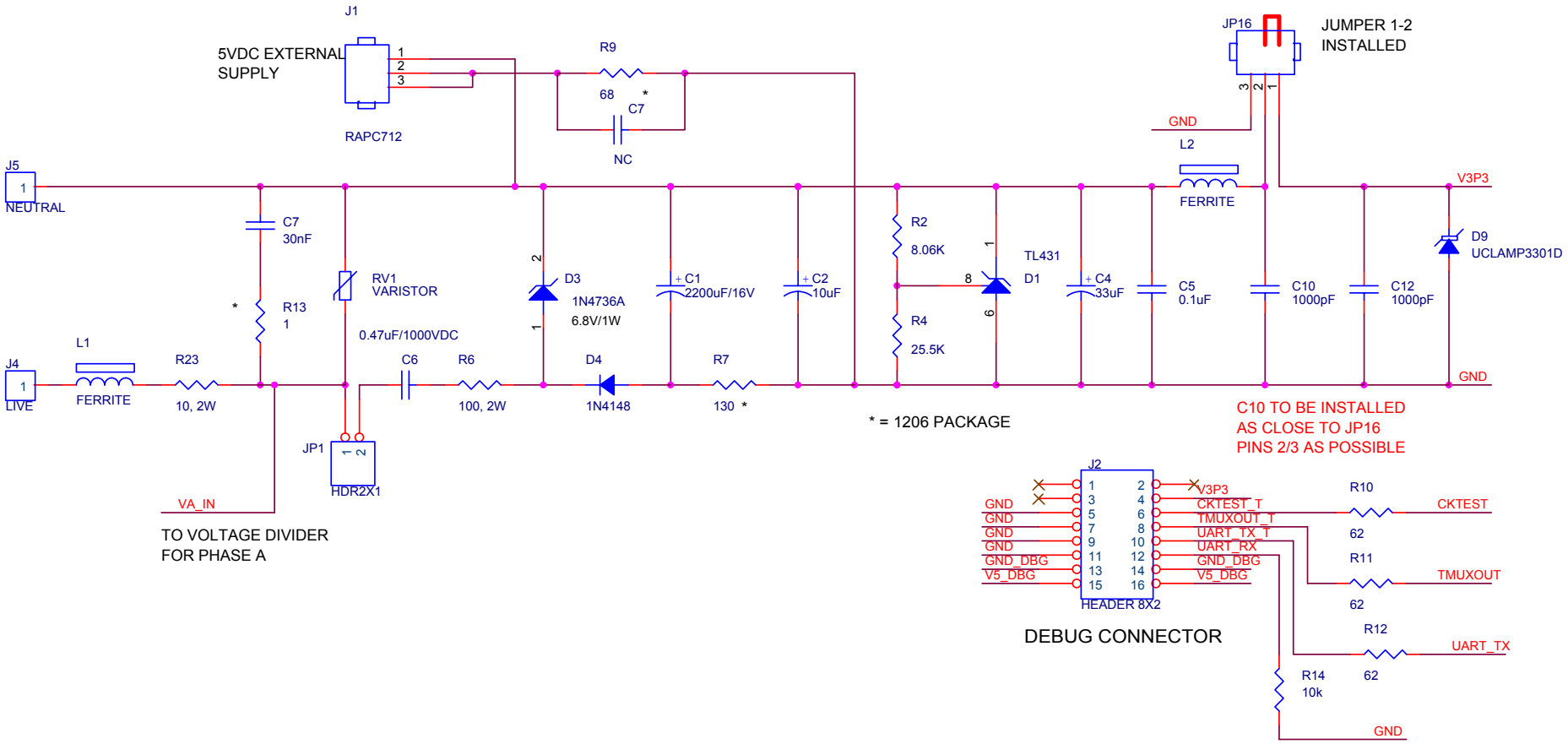


Figure 10: Schematics (1/3)

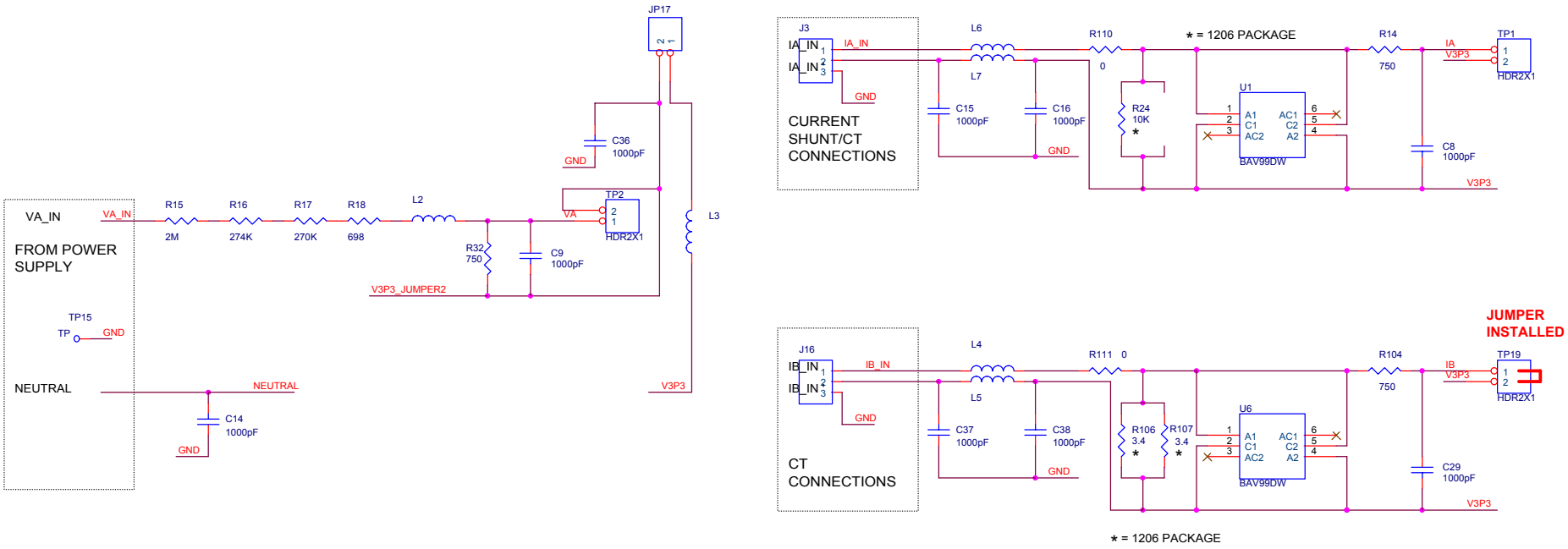


Figure 11: Schematics (2/3)

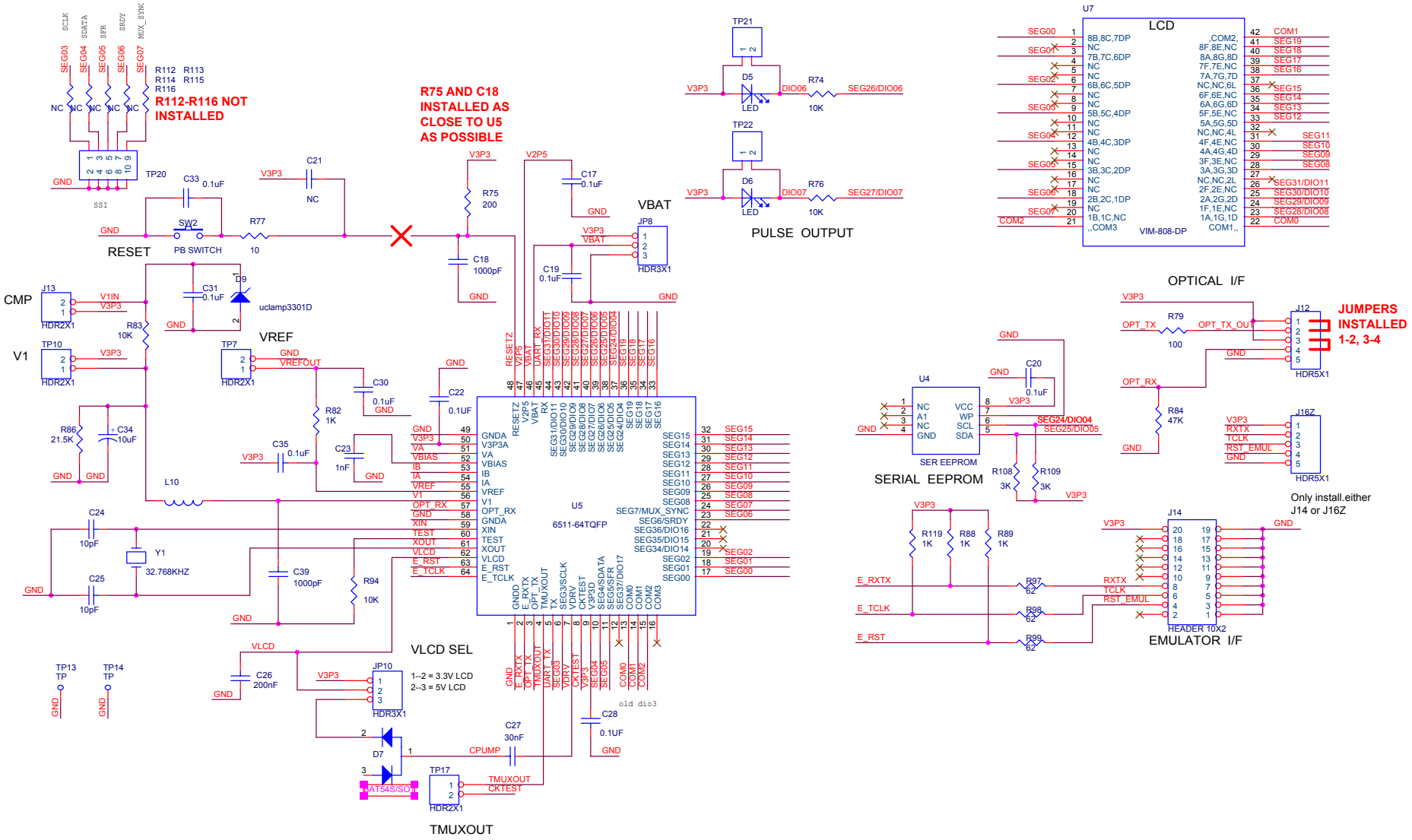


Figure 12: Schematics (3/3)

Enclosure Design

Care must be taken to ensure that the meter design is not ESD sensitive. When a shielded meter enclosure cannot be used, sufficient spacing (12.5mm) must be provided between the enclosure perimeter and the electrically sensitive parts of the meter PCB.

The design described in this application note had not been optimized for ESD. Thus, a slightly larger enclosure than necessary was used in order to provide the clearance needed for ESD testing (see Figure 13).

Figure 13: Demo Board in Enclosure

This product is sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement and limitation of liability. TERIDIAN Semiconductor Corporation (TSC) reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders. TSC assumes no liability for applications assistance.

TERIDIAN Semiconductor Corp., 6440 Oak Canyon Rd., Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

© 2004-2005 TERIDIAN Semiconductor Corporation 9/22/05 – REV 2.0