AN_651X_016

APPLICATION NOTE

MARCH 2006

EMC/EMI Design Guidelines for 71M651x ICs

Designing a meter for optimum electromagnetic compatibility can be a challenging issue for any design engineer. EMC/EMI testing for metering products involve the Conduced and Radiated Emissions, RF Immunity, Electro-static Discharge (ESD) and Electrical Fast transient (EFT) testing. Successfully passing these tests depends on many factors, such as schematic design, PCB design, component selection, component placement on the PCB and the input connections of the current sensing elements to the meter. The methods presented in this document provide EMI suppression without affecting accuracy performance of the meter.

Following the recommendations outlined in this document in the initial phase of schematic and PCB design helps generating EMI/EMC compliant designs up front, avoiding potential rework of PCBs.

This document describes the details for EMI/EMC compliance based on 71M651x Demonstration Boards.

Note: Reference designators are given in a generalized form and do not necessarily relate to the reference designators used on actual TERIDIAN Demo Boards.

Schematic Design Precautions

In this section, details of schematic design for critical areas of the meter will be discussed.

Current Inputs:

71M651x devices accept three commonly used current sensor inputs such as

a. Current Transformers

b. Current Shunts

c. Rogowski Coils

Displayed and recorded energy under EMI conditions depends on the design of the current and voltage inputs. Improper design may lead to erroneous display of energy, especially in cases where loads are disconnected, as required by some test standards.

The input signal conditioning circuits depend on the current sensors used and are described in detail in the following sections.

Current Transformers

Figure 1shows the suggested input signal conditioning circuit.

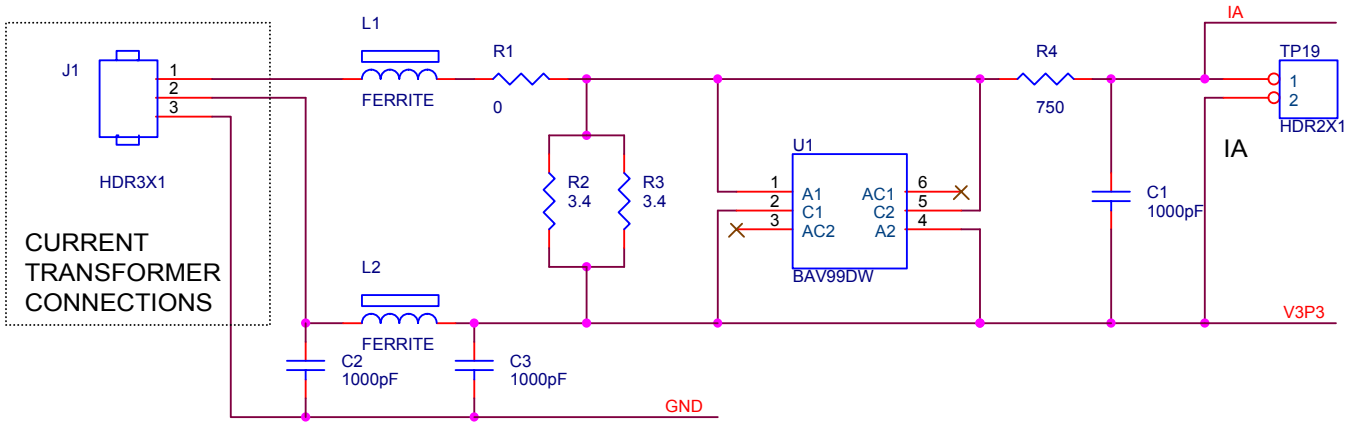

Figure 1: CT Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. The combination of R4 and C1 provides a low pass filter for differential signals with cutoff frequency of around 212kHz.
3. Connector J1 has a third pin provision (some Demo Boards use only two of those pins). Connect pin3 of J1 to the shield of the CT cable if needed.
4. R1 is 0Ω.
5. The combination of C2, L2, and C3 eliminates high-frequency noise spikes on the analog reference, V3P3.

Current Shunt

Figure 2 shows the suggested input signal conditioning circuit for Current Shunt inputs.

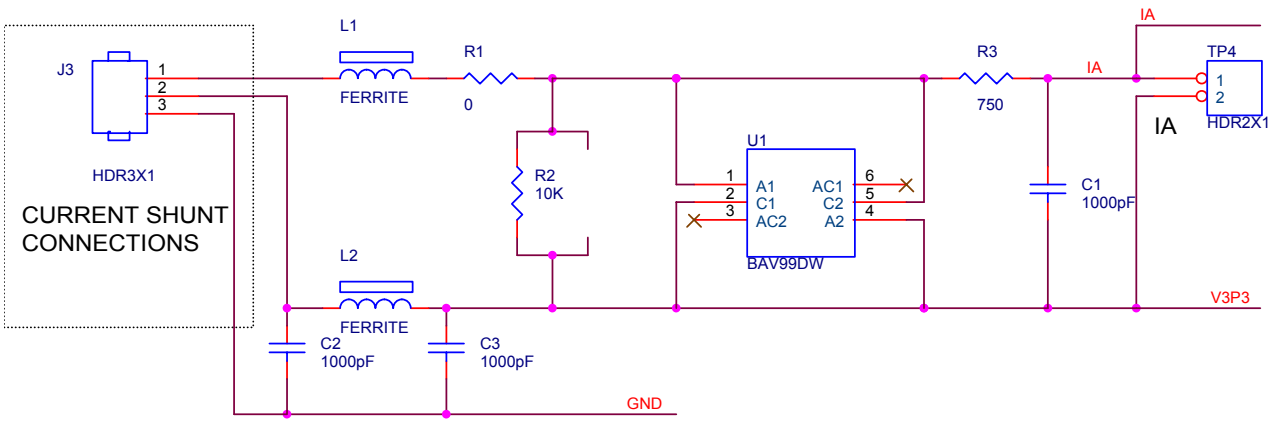

Figure 2: Current Shunt Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. Generally, the Current Shunt interface to 71M6511 Demo Boards involves a four-wire connection. Two of the wires connect as shunt inputs for the current sensing circuit and the other two wires are tied to one side of the shunt along with one of the one current sensing wire. These two wires may also need to be shielded and the shield should then be connected to digital ground of the PCB.
2. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
3. R3 and C1 provide a low pass filter for differential signals. Depending on the length of the cable harness used to hook up the current shunt, the value of the capacitor C1 may vary.
4. Connector J3 has a third pin provision to accommodate for the connection to the shield of the Shunt cable to connect to the digital ground to prevent high frequency noise entering through the Shunt metal plate and the connecting cables.
5. C2, L2 and C3 form a Pi-filter that eliminates high-frequency noise spikes on the analog reference, V3P3.
6. R2 is basically in parallel to the Shunt Resistor and is used to eliminate noise.
7. R1 is 0Ω.

Note: Some EMI suppression components are not available on the 4-Layer 6511 Demo Board.

Rogowski Coil

Figure 3 shows the suggested input signal conditioning circuit for Rogowski coils.

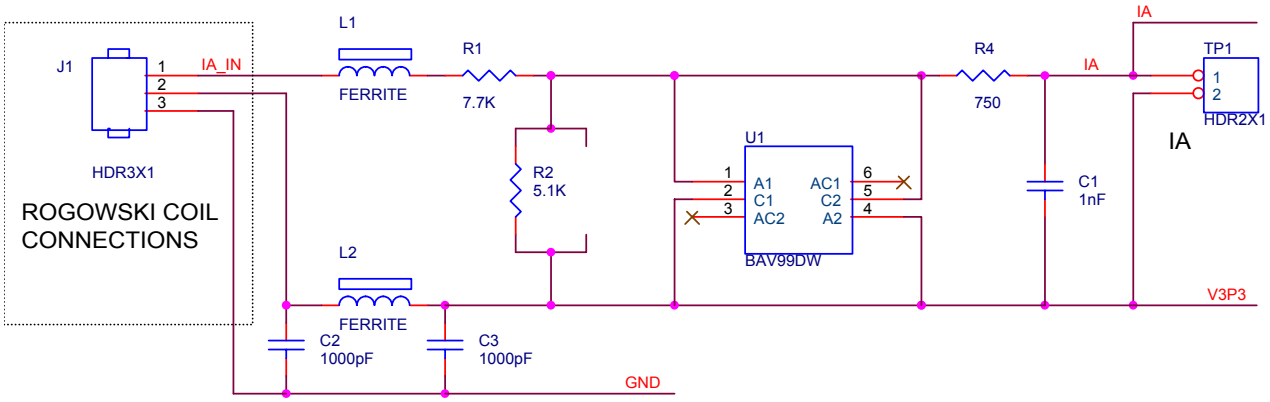

Figure 3: Rogowski Coil Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. L1 and L2 are Ferrite beads that provide 600-Ohm impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. R4 and C1 provide a low pass filter for differential signals with cutoff frequency of around 212kHz.
3. Connector J1 has a third pin provision to accommodate the connection of the cable shield if there is a necessity to use shielded cable. If used, the shield needs to be connected to digital ground.
4. C2, L2 and C3 form a Pi-filter that eliminates high-frequency noise spikes on the analog reference, V3P3.

Sensor Wiring

The following precautions apply to sensor wiring:

1. Sensor wires may be shielded. This applies especially to sensor wiring used in the Shunt Resistor configuration. Inside the shield, the wires should be twisted (STP).
2. If used, shields for sensor wiring should be terminated to DGND. Some Demo Boards have provisions for connecting the shield wire.
3. If shielding is not desired, unshielded twisted wire (UTP) pairs may be used.
4. Sensor wires should be kept as short as possible.
5. Ferrites may be used on sensor wiring to prevent common-mode noise.

Power Supply Circuit

Figure 4 shows the suggested power supply circuit (power supply with capacitive coupling). In general, power supplies using transformers will provide better results in EMC/EMI testing.

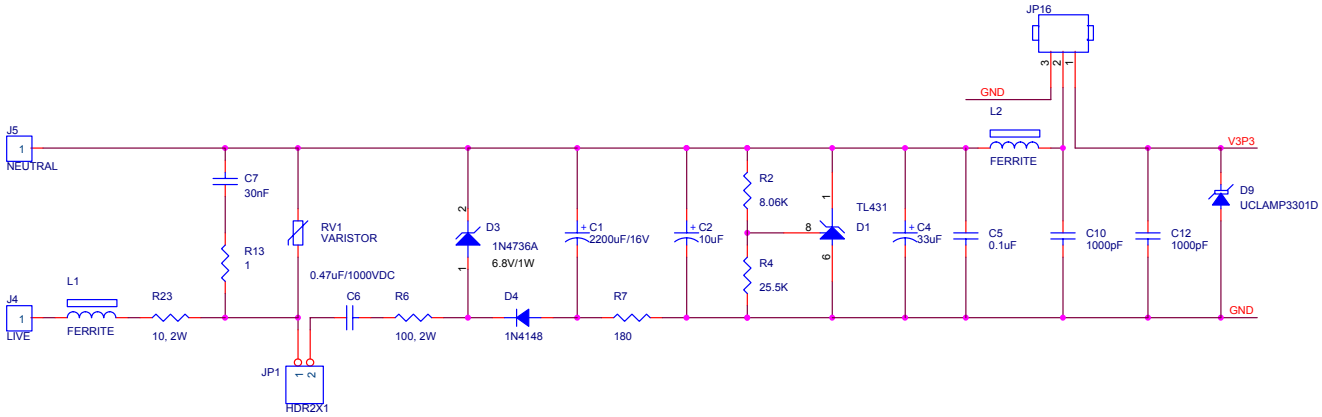

Figure 4: Power Supply Circuit

Key precautions recommended for the power supply circuit are:

1. The Ferrite bead L2 at the V3P3 output prevents high frequency noise.
2. A TVS (Transient Voltage Suppressor D9) is added to clamp the V3P3 supply voltage to 3.3V. This device may be a bi-directional clamping device to prevent high voltage peaks into the circuit, e.g. the SEMTECH UCLAMP3301D.
3. The resistor R23 is added in series to the varistor (MOV) to limit the surge current. This resistor will cause a voltage drop that helps protecting both the varistor and the meter circuitry. The resistor may be a flame-proof 10Ω type rated 3W to 5W.
4. The high-voltage capacitor C7 is added in parallel to the varistor to suppress high-frequency noise. The series resistor R13 (1Ω) is used to dampen oscillations that may occur due to the effective impedance of the power supply.
5. C10 and C12 suppress high-frequency noise.

Voltage Inputs (CT Mode)

Figure 5 shows a typical voltage input circuit. Key precautions are:

1. L1 is a Ferrite bead that provides 600-Ohm impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. R1+R2+R3+R4 and C1 provide a low pass filter for differential signals.
3. The highest value of the resistor ladder (in this case R1) should be placed directly at the voltage input. This will result in the highest voltage drop. Consequently, the voltages at R2, R3, etc. will be in a safer range, and precautions for leakage or arching need only be taken for R1.
4. C2 filters noise on the Neutral connection. C2 appears as C14 on many Demo Boards.
5. On the 6511 Demo Boards, JP17 is shorted with a jumper to provide a path from V3P3 at the 6511 IC to the analog reference (A_REF).

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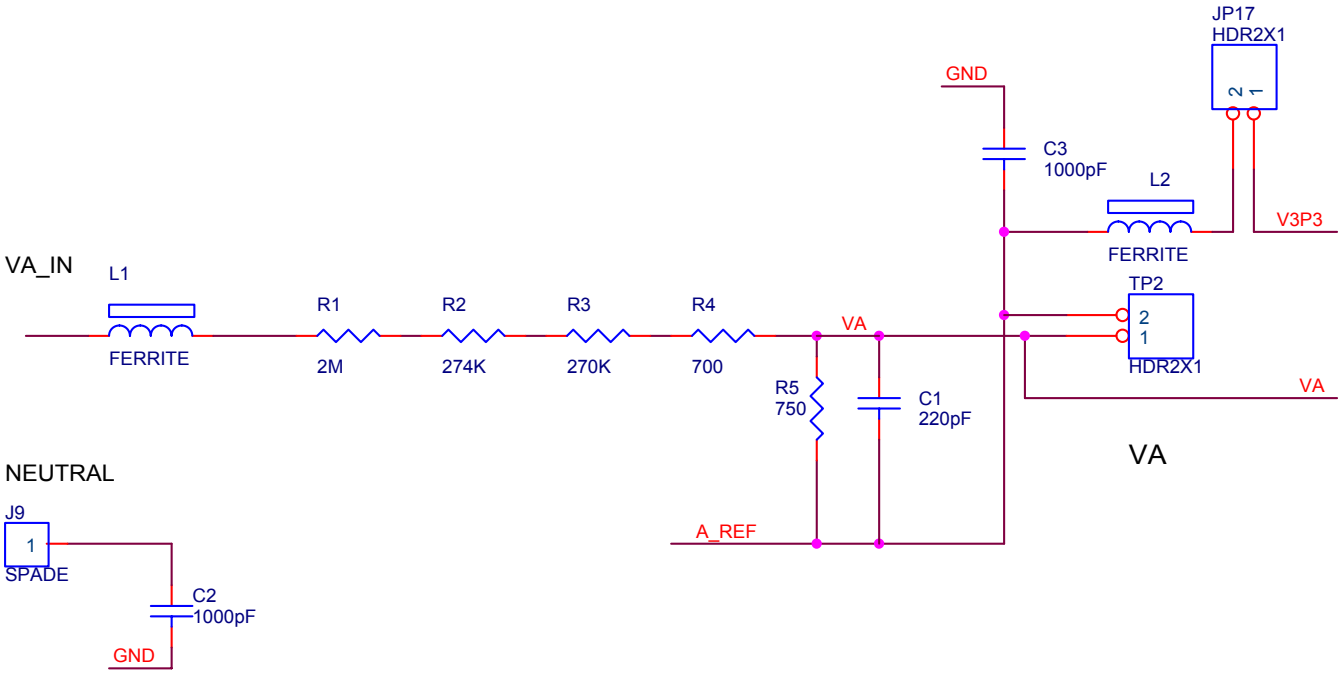

Figure 5: Voltage Input Circuit for CT

Voltage Inputs for Current Shunt Mode

Figure 6 shows the circuit to be used when a 6511 Board is operated in current shunt mode. When using the Demo Boards, JP17 is left open and one of the three wires coming from the line side of the current shunt will connect to JP17, pin 2. C3 and L2 have been added for noise protection of this signal. Capacitor C2 in Figure 6 appears as C14 on the Demo Boards.

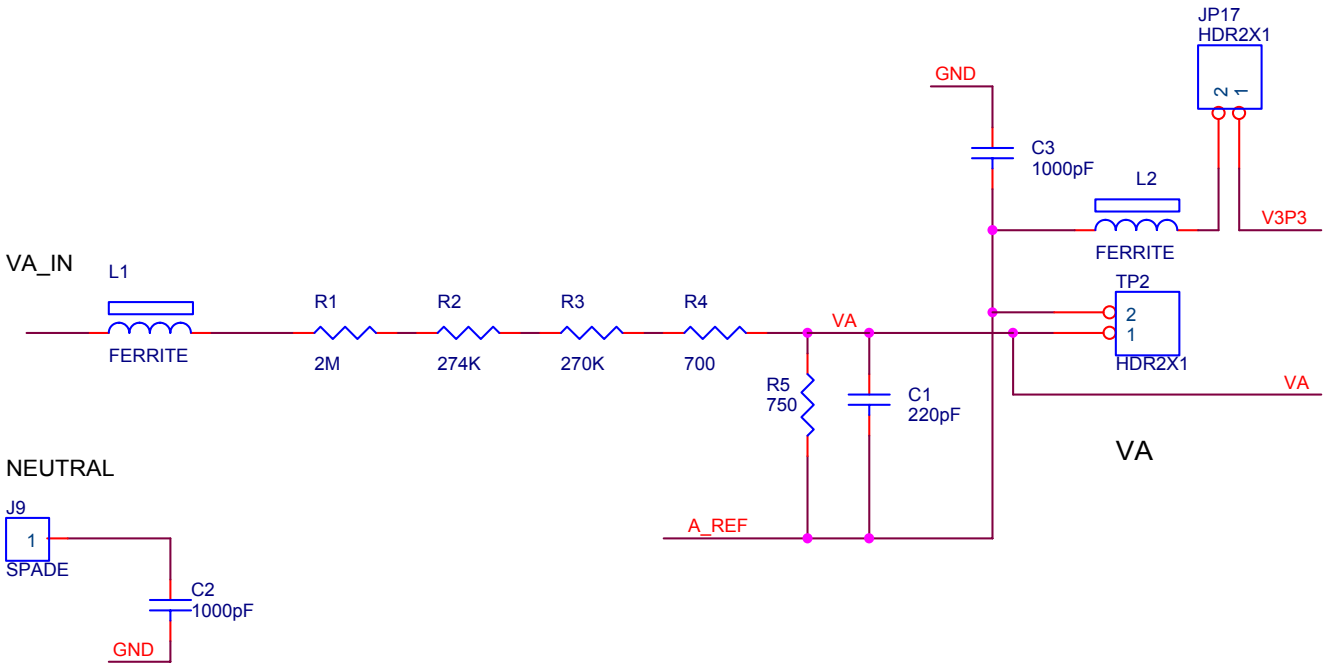

Figure 6: Voltage Input Circuit for Current Shunt Mode

Reset Circuit

The RESETZ pin of the 651X tends to pick up noise when not properly terminated. Long traces leading to the RESETZ pin must be avoided.

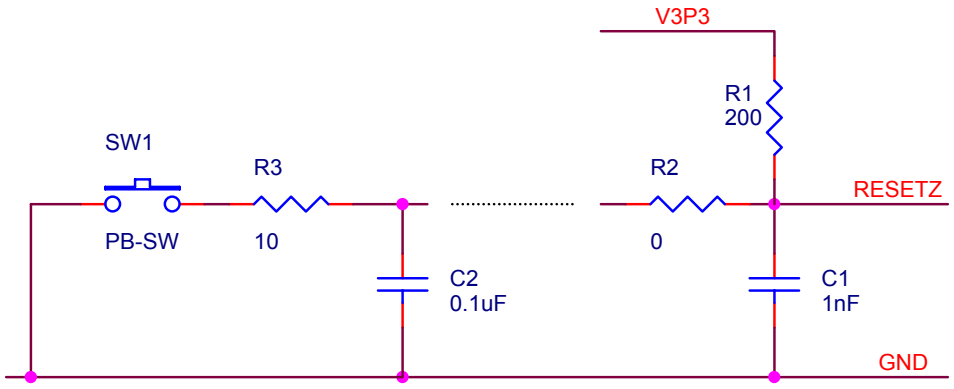

Figure 7: Reset Circuit

It is beneficial to terminate the RESETZ signal very close to the 651X chip with a strong pull-up resistor and a small capacitor (R1 and C1 in Figure 7). If the reset pushbutton cannot be located right at the chip, another resistor (R2) should be provided between the RESETZ net and the switch. Removing this resistor will separate the switch from the RESETZ pin to ensure proper function in severe EMI/EMC environments.

Emulator Reset (E_RST)

The E_RTS pin of the 651X demands the same attention that is paid to the RESTEZ pin. Long traces leading to the E_RTS pin must be avoided. A capacitor to ground close to the E_RST pin at the chip should be added.

V1 Circuit

V1 is the power fault input to the 651X IC. It tends to pick up noise when not properly terminated. Any disturbance reaching this pin (e.g. from sensors connected to V3P3) can potentially drive the IC into reset. Long traces leading to the V1 pin must be avoided.

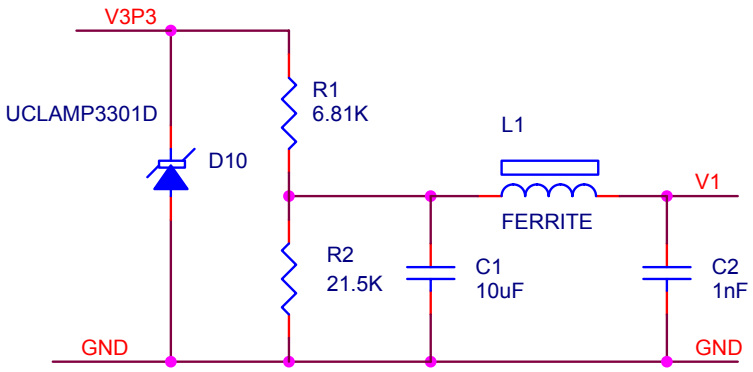

Figure 8: V1 Circuit

V1 should be decoupled with a 10µF tantalum capacitor to ground and held close to 2.5VDC, e.g. by a voltage divider of 6.81kΩ/21.5kΩ. The capacitor C2 (in Figure 8), in conjunction with the ferrite L1, helps eliminating high-frequency noise. Adjusting V1 too low can have the effect that short sags of the V1 voltage could drive the IC into reset.

Other 651X IC Signal Pins

All signals from and to the 651X IC have to be carefully examined for EMI susceptibility. Careful termination helps to defeat unwanted resets or false readings caused by RF fields.

Following are the precautions for the other IC pins on the demo board/ 71M651X:

1. Signal input pins (**IA, IB, IC, VA, VB, VC**): All unused current and voltage inputs should be tied to V3P3.
2. A 10µF tantalum capacitor should be used between the **V3P3A** pin of the IC and ground. It should be mounted as close as possible to the 651X IC (C18 on the Demo board)
3. The **VREF** pin should be bypassed with a 0.1µF capacitor to ground and another 0.1µF capacitor to V3P3.

4. Any unused signal nets should be cut and terminated as closely to the IC as possible. For the Demo Board this means that the switch SW1, R100 through R102, R112 through R116, and all connections to the debug connector should be removed.
5. A 0.1µF capacitor should be placed between the **V2P5** pin and ground. This improves the operation of the internal regulator used to generate 2.5VDC from 3.3VDC by reducing ripple.
6. Strong pull-up resistors (1kΩ) should be used for the emulator signals (**E_RST, E_TCLK, E_TXRX**) in order to support the relatively weak internal pull-up resistors in the IC.
7. Pins **OPT_TX** and *OPT_RX*, when not used, should be tied to V3P3.
8. Unused SSI/segment pins should be disabled on the Demo Boards by removing the resistors R112-R116.
9. When no battery is used, the **VBAT** pin should be tied to V3P3.

Layout Precautions

1. The most successful layouts use four layers, with the two internal layers being ground and V3P3.
2. If two-layer boards are used, the layout has to be designed very carefully:
   - It is helpful to keep the high-voltage and low-voltage sections of the board clearly separated.
   - Ground and V3P3 traces should be widened (using copper pour techniques) to become virtual planes. Naturally, it is impossible to route a 2-layer board with continuous copper planes. However, ground and V3P3 structures can be placed on both sides of the board and then “stitched” together with free vias, creating good connectivity for both V3P3 and ground.
   - For a good example of a two-layer board, examine the 6511 2-Layer Demo Board (see Figure 10 and Figure 11).
3. The V3P3A plane for measurement should be wide enough to act as a stable reference for the measurement signals. The wider the V3P3A copper structure is, the better the measurement performance of the meter will be. All V3P3 structures should come together at a star point close to the V3P3A pin of the IC.
4. The crystal should be positioned as close as possible to the 71M651x IC and rotated properly to make the traces short. No other traces should cross the traces between the IC and the crystal on the other side of the board. The parallel resistor implemented in some Demo Boards is not needed.
5. Slots cut into the PCB should be used for isolation where high-voltage signals are located close to low-voltage signals. This prevents arching or leakage currents when the PCB surface is not perfectly clean.
6. When laying out the V3P3 traces, a “Kelvin” junction scheme should be used, i.e. all connections should meet at a star point close to the V3P3 pin of the IC.
7. It is unrelated to EMI (but very important none the less) when using the 71M6513 chip, to make sure that no traces or vias are located in the area that is covered by the 5mm x 5mm exposed ground pad (for an example, see Figure 9, showing routing patterns that are not recommended).

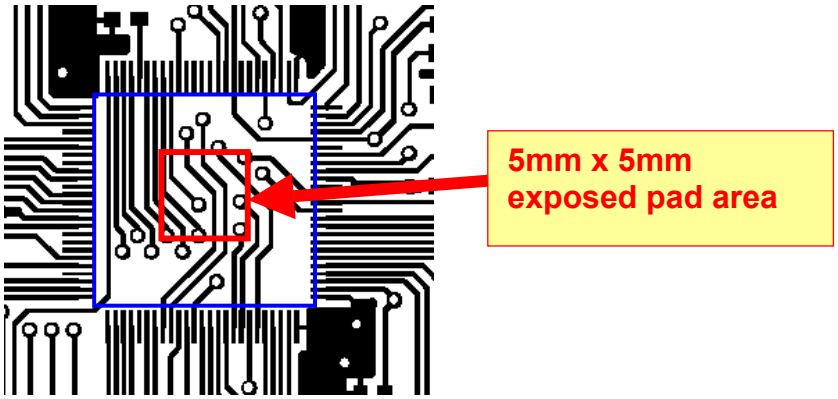

Figure 9: Problematic Routing underneath 71M6513 Chip

Firmware/Configuration Precautions

1. All unused DIO pins should be configured as outputs. This way no unwanted signals enter the IC.
2. The emulator clock should be disabled (by configuring *ECK_DIS* to 1) so that no 5MHz clock (I/O RAM 2005 Register Bit 5) is generated at the emulator port. This prevents any emissions due to the 5MHz clock signal. This also ensures that the emulator port is disabled.
3. The RTM clock output should be disabled (by configuring *CKOUT_DIS* to 1) when no Real-Time monitoring is performed with the production version of the firmware.
4. Dummy interrupt service routines containing a RETI instruction should be placed at all locations pointed to by unused interrupt vectors.
5. All interrupt service routines (ISRs) should be as short as possible and should be minimized for memory manipulation operations.

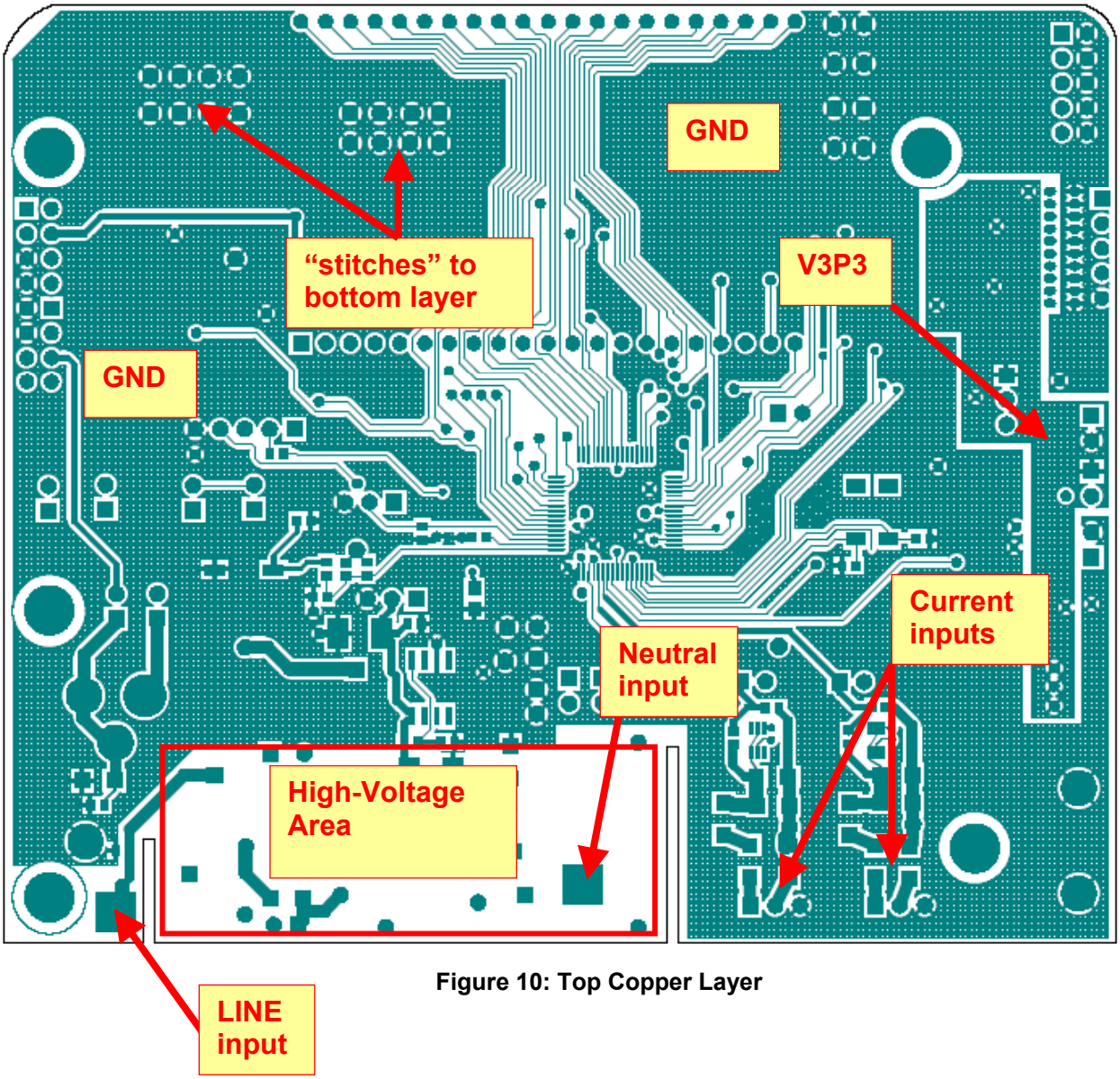

Figure 10: Top Copper Layer

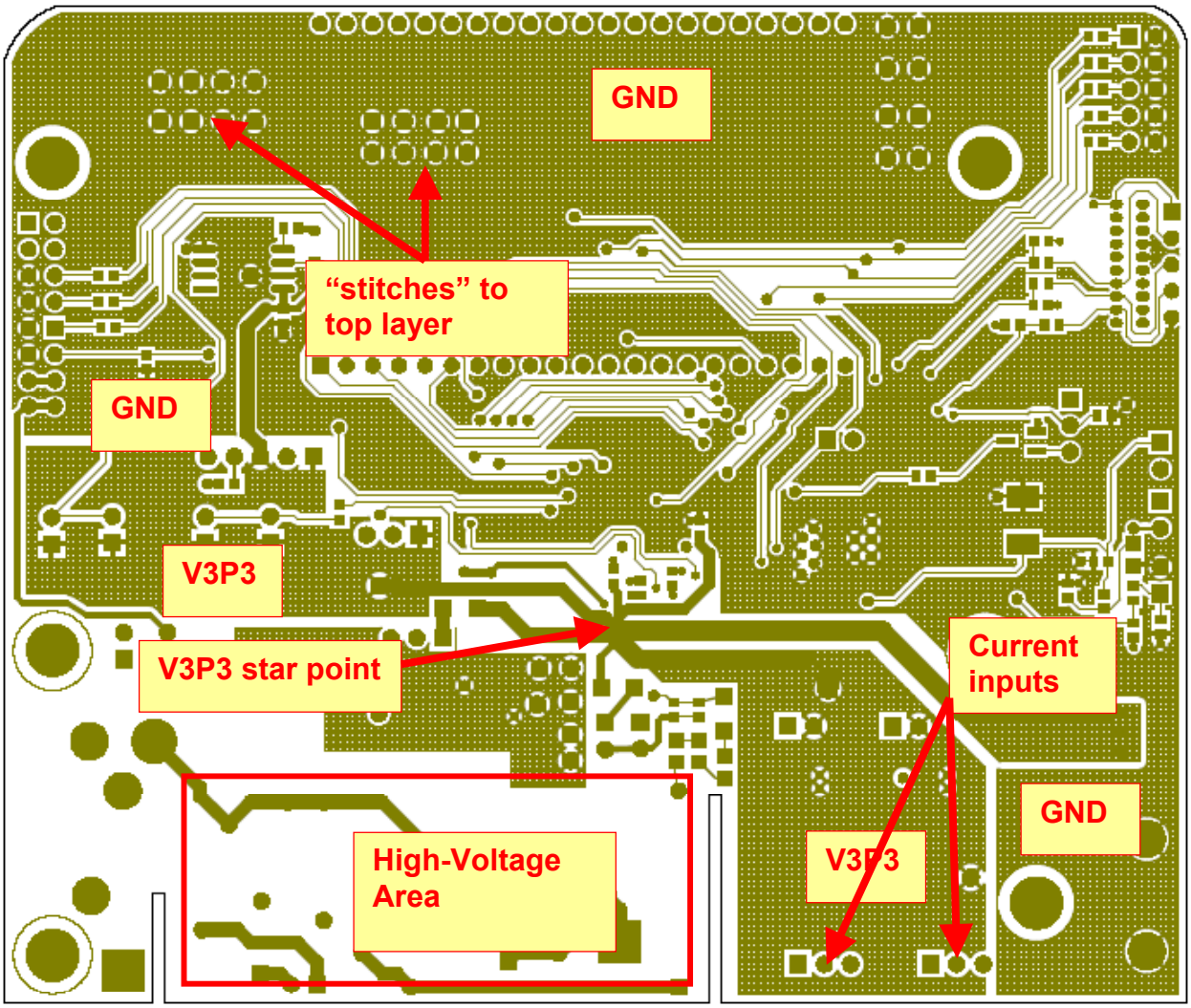

Figure 11: Bottom Copper Layer

External Components

In some cases, some external components may have to be added to pass EMI/EMC testing. If careful layout and component selection do not yield the expected result, ferrites can be added to the sensor and other external wiring.

Figure 12 shows a 6511 2-Layer Demo Board modified to pass **30V/m RF** immunity testing.

A large clamp-on ferrite (1) is used for the power-entry cable, and two smaller clamp-on ferrites (2) are attached to the Shunt Resistor wiring. Another small toroid ferrite (3) is attached to the power-entry wire to the board.

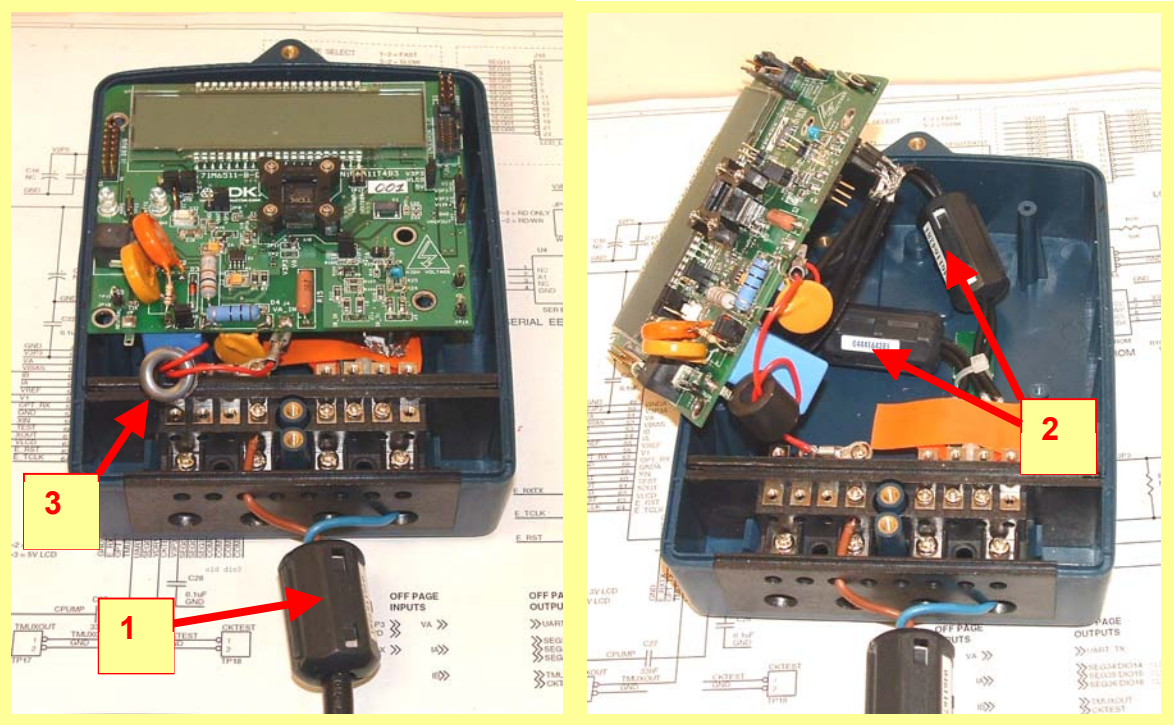

Figure 12: 6511 2-Layer PCB with external components

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