AN_6521_049

APPLICATION NOTE

February 2008

Transition from the 71M6521 to the 71M6521xE

Introduction

The energy metering ICs 71M6521FE, 71M6521DE and 71M6521BE are now available from TERIDIAN. This Application Note describes the main differences between the 71M6521xE and the 71M6521 and provides details on the changes in software required when replacing the 71M6521 in an existing design with the 71M6521xE.

Main Differences

Based entirely on the proven 71M6521, the 71M6521xE offers the following improvements:

1. The IC offers improved resistance against ESD and EFT.
2. The on-chip temperature sensor was modified to remove variation with changes in power supply. This modification results in a changed LSB value of the temperature sensor.
3. Yield enhancement for -40ºC crystal oscillator startup.
4. Yield enhancement for bias startup circuit with a slow ramping supply.

All changes above were performed with metal layers only.

Changes 1 and 2 will be discussed further in this Application Note.

The 71M6521xE is a pin-compatible replacement for the 71M6521.

ESD and EFT Performance

ESD and EFT performance of an electricity meter are primarily a function of board layout, wiring, sensor types, and choice of protective components. Direct comparisons of identical Demo Boards containing the 71M6521 and the 71M6521xE have shown a significant improvement of the 71M6521xE over the 71M6521.

The TERIDIAN D6521T12A3 Demo Board with standard Demo Code was used to test both the 71M6521 and the 71M6521xE chips to exceed IEC 61000-4-2.

In separate tests, ten manual air discharges over a 1 mm distance to the horizontal discharge plate (method frequently used in China) were applied at each voltage level starting from 1 kV and increased at 100 V intervals using the ESD tester model ESS2000 (manufactured by NoiseKen, Japan) until a reset was observed. The results (i.e. passing voltages with no malfunction) are summarized in Table 1.

Test Type	6521 (68QFN)	6521xE (68QFN)
Air discharge	16 kV	30.0 kV

Table 1: ESD Performance (68-pin Package)

EFT immunity performance was tested on Demo Boards to allow a direct comparison between 71M6521 and 71M**6521xE** chips.

The TERIDIAN D6521T4A7 Demo Board with shunt connection in a sample meter enclosure and standard Demo Code was used to test both the 71M6521 and the 71M**6521xE** chips for EFT immunity with the model NSG2025 EFT tester (manufactured by Schaffner, Switzerland). The double sequence 4 kV test routine was extended to 8 kV. The results (i.e. passing voltages with no malfunction) are summarized in Table 2.

Test Type	6521	6521xE
LIVE	5.7 kV	7.8 kV
NEUTRAL	5.3 kV	6.2 kV

Table 2: EFT Performance

Despite the improved ESD and EFT performance of the 71M**6521xE**, good schematic and layout practices should be applied when designing meters.

Temperature Sensor Output

Specifications

With the transition from the 71M6521 to the 71M**6521xE**, the slope of the temperature sensor, i.e. the LSB value of the ADC reading per degree C changed to the values shown in Table 3. The values depend on the length of the FIR filter (determined by the I/O RAM register *FIR_LEN*) used for the ADC.

***FIR_LEN* Setting**	**71M6521xE**	**71M6521**
	Slope [LSB/°C]	**Slope [LSB/°C]**
FIR_LEN = 1	-2180	-1100
FIR_LEN = 0	-918	

Table 3: Temperature Sensor Slope

It should also be noted that changes in supply voltage will not affect the output of the temperature sensor of the 71M**6521xE**, as can be seen in Figure 1. The numbers for Figure 1 were obtained by measuring the output of the temperature sensor (raw output = 2 times averaged output) over the temperature range from –40°C to +85°C at several different supply voltages, 3.1 V, 3.3 V and 3.5 V.

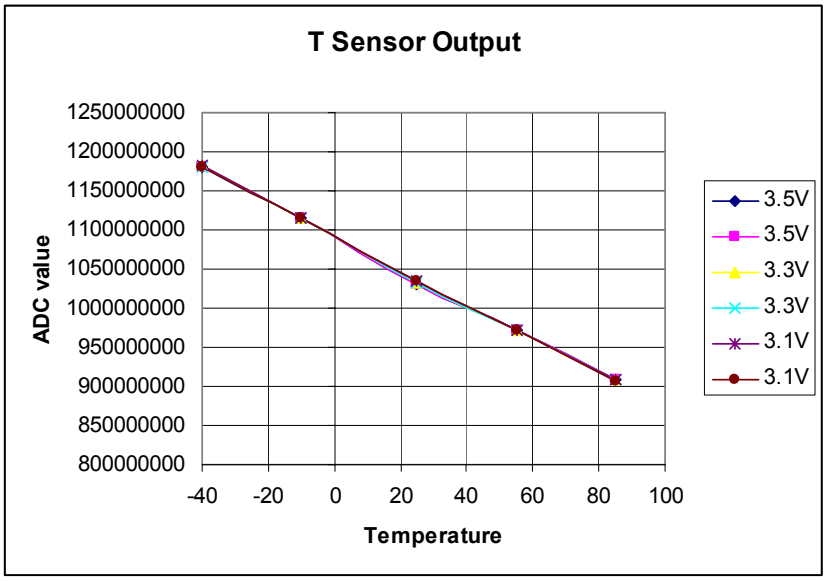

Figure 1: Temperature Sensor Output

Potential Firmware Changes

The change in temperature sensor slope is only an issue if the meter implemented with the 71M**6521xE** utilizes at least one of the following functions:

1. Temperature measurement (display, recording or reporting of temperature relative to calibration temperature).
2. Compensation of energy measurements over temperature.
3. Compensation of the RTC over temperature (71M6521DE and 71M6521FE only).

Depending on the setting of *FIR_LEN*, the firmware has to apply the proper slope, as specified in Table 3, when determining chip temperature.

Temperature Measurement

Measurement of absolute temperature uses the on-chip temperature sensor while applying the following formula:

$$T = \frac{(N(T) - N_n)}{S_n} + T_n$$

In the above formula T is the temperature in °C, N(T) is the ADC count at temperature T, N_n is the ADC count at 25°C, S_n is the sensitivity in LSB/°C as stated in Table 3, and T_n is +25°C.

Example: At 25°C a temperature sensor value (N_n) of 518,203,584 is read by the ADC in a 71M6521FE (64-pin LQFP) with *FIR_LEN* set to 1. At an unknown temperature T, a sensor value, N(T), of 449,648,000 is read. The absolute temperature is then determined by dividing both N_n and N(T) by 512 to account for the 9-bit shift of the ADC value (N_n/512 = 1,012,116, N(T)/512 = 878,219) and then inserting the results into the above formula, using –2180 for the slope (LSB/°C):

$$T = \frac{878{,}219 - 1{,}012{,}116}{-2180} + 25C = 86.4C$$

Compensation of Energy Measurements and RTC over Temperature

The temperature coefficients TC1 and TC2 are given in the data sheet as constants that represent typical component behavior (in µV/°C and µV/°C^2, respectively). Since TC1 and TC2 are given in µV/°C and µV/°C^2, respectively, the value of the VREF voltage (1.195 V) has to be taken into account when transitioning to PPM/°C and PPM/°C^2.

For the purpose of temperature compensation, the CE provides the bandgap temperature to the MPU in the form of ADC readings, which then digitally compensates the power outputs for the temperature dependence of VREF, using the CE register *GAIN_ADJ*.

For the 71M6521DE and 71M6521FE, the MPU, not the CE, is entirely in charge of providing temperature compensation. *DELTA_T* (expressed in multiples of 0.1°C) should be derived from the temperature sensor output using the following formula:

$$DELTA\_T = 10 \cdot \frac{(N(T) - N_n)}{S_n}$$

The MPU then applies the following formula to determine *GAIN_ADJ* (CE address 0x12).

$$GAIN\_ADJ = 16385 + \frac{DELTA\_T\_X \cdot PPMC}{2^{14}} + \frac{DELTA\_T^2 \cdot PPMC2}{2^{23}}$$

Revision History

Revision	Date	Description
October 2007	10/19/2007	First publication.
January 2008	1/31/2008	Changed temperature slope value to –2180/C for both package types. Updated Figure 1. Removed reference to engineering samples availability. Add yield enhancement change description.
February 2008	2/13/08	Clarified ESD performance.

Teridian Semiconductor Corp., 6440 Oak Canyon Rd., Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com