TERIDIAN SEMICONDUCTOR CORP.

71M652X Power Meter IC

AN_652X_001

APPLICATION NOTE

MARCH 2007

EMC/EMI Design Guidelines for Meters Using 71M652X ICs

Design for electromagnetic compatibility (EMC) must be a top priority from the beginning of the design cycle. Routine EMC/EMI tests for metering products typically include:

- Conducted and Radiated Emissions tests
- RF Immunity tests
- Electrostatic Discharge (ESD) tests
- Electrical Fast transient (EFT) tests

Successfully passing these tests depends on many factors, including:

- Functional operation (schematic design)
- Printed circuit board topology and component & signal trace placement (PCB design)
- Component selection
- Input connections of the sensing elements to the meter
- Firmware program

The methods presented in this document are incorporated into the TERIDIAN Demo Boards enhancing EMI compatibility without affecting accuracy performance of the meter.

Following the recommendations outlined in this document in the initial phase of schematic and PCB design helps generating EMI/EMC compliant designs up front, avoiding potential rework of PCBs.

Note: Reference designators are given in a generalized form and do not necessarily relate to the reference designators used on actual TERIDIAN Demo Boards.

Current Inputs

71M652X devices accept three commonly used current sensor inputs.

- Current Transformers
- Current Shunts
- Rogowski Coils

Accurate display and recording of energy under EMC conditions depends on the design of the current and voltage inputs. Improper design may lead to erroneous display of energy. Disconnection of loads, as required by some test standards can be extremely troublesome.

The input signal conditioning circuit depends on the type of current sensor used. Each of the three current sensor types are individually discussed in this section.

Current Transformers

Figure 1 shows the recommended input signal conditioning circuit.

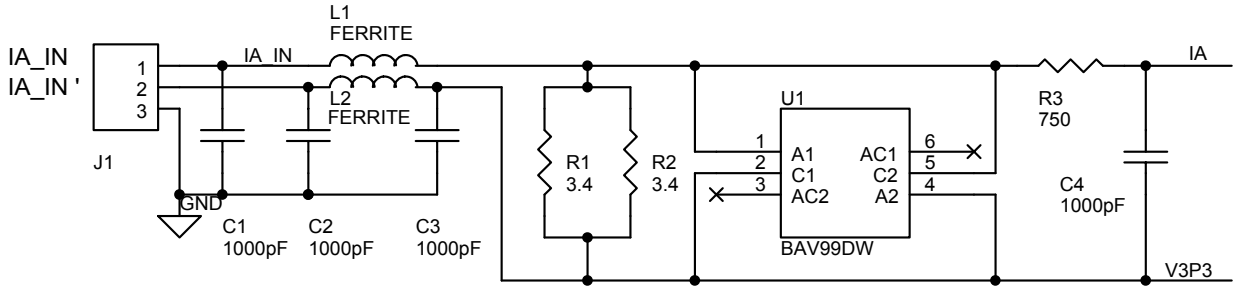

Figure 1: CT Input Signal Processing Circuit

Key recommendations for passing EMC/EMI testing for the CT input signal conditioning circuit:

1. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (use TDK MMZ2012S601A or equivalent).
2. The combination of R3 and C4 provides a low-pass filter for differential signals with a cutoff frequency of around 212kHz. Depending on the length of the sensor cable harness, the value of C4 may vary.
3. Connector J1 has a third pin for GND connection. Connect pin 3 of J1 to the shield of the CT cable (if available) to minimize high-frequency noise entering through the sensor cable.
4. The combination of C2, L2, and C3 eliminates high-frequency noise spikes on the analog reference signal V3P3.

Current Shunt

Figure 2 shows the recommended input signal conditioning circuit.

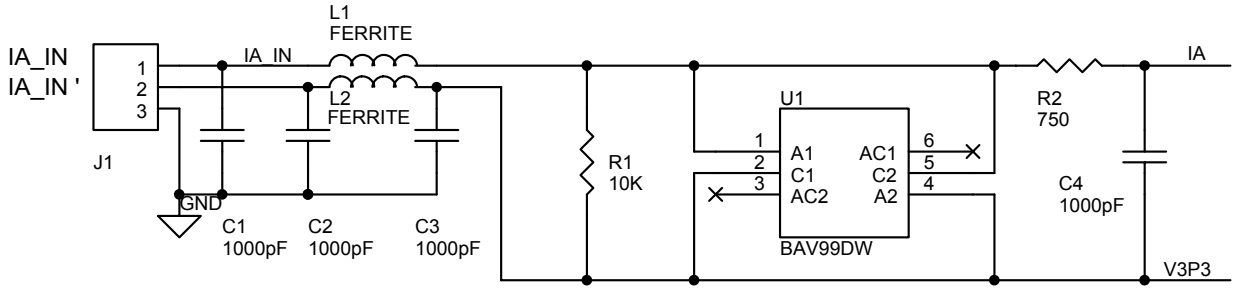

Figure 2: Current Shunt Input Signal Processing Circuit

Key recommendations for passing EMC/EMI testing for the current shunt input signal conditioning circuit:

1. The current shunt assembly provided with the 71M652X Demo Boards involves a four-wire connection. Two of the current shunt assembly wires connect to J1 as shunt inputs for the current sensing circuit. The other two wires attached to one side of the current shunt provide additional Neutral connections to the Demo Board.
2. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (use TDK MMZ2012S601A or equivalent).
3. R2 and C4 provide a low pass filter for differential signals with a cutoff frequency of around 212kHz. Depending on the length of the sensor cable harness, the value of C4 may vary.
4. Connector J1 has a third pin for GND connection. Connect pin 3 of J1 to the shield of the shunt cable (if available) to minimize high-frequency noise entering through the shunt sensor plate and the sensor cables.
5. The combination of C2, L2, and C3 eliminates high-frequency noise spikes on the analog reference signal V3P3.
6. R1 acts as a damping resistor in parallel with the current shunt to minimize EMI noise.

Voltage Inputs

Voltage inputs for CT mode and for current shunt resistor mode are available on the 652X Demo Boards.

Voltage Inputs (CT Mode)

Figure 3 shows the recommended input circuit when using a current transformer.

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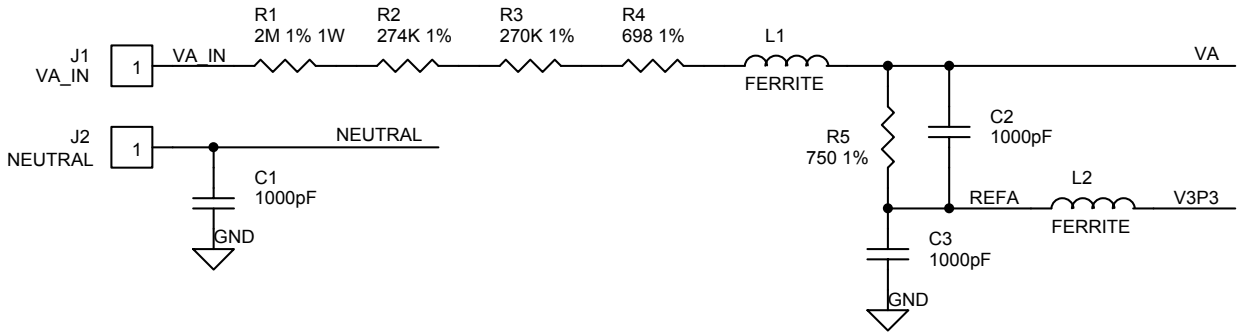

Figure 3: Voltage Input Circuit for CT

The recommendations for the design of the CT input signal conditioning circuit with respect to EMC/EMI testing are:

1. L1 and L2 are Ferrite beads that provide 600-Ohm impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. R1+R2+R3+R4 and C2 provide a low pass filter for differential signals.
3. The highest value of the resistor ladder (in this case R1) should be placed directly at the voltage input terminal. This component experiences the highest voltage drop. Consequently, the voltages at R2, R3, etc. will be in a safer range and precautions for leakage or arching need only be taken for R1.
4. C1 filters EMI noise on the Neutral connection.

Voltage Inputs for Current Shunt Mode

Figure 4 shows the recommended voltage input circuit when using a current shunt.

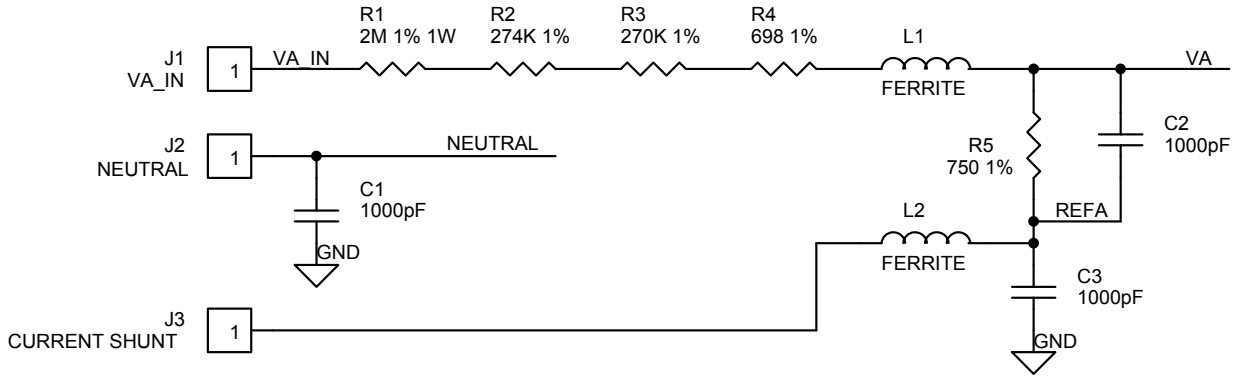

Figure 4: Voltage Input Circuit for Current Shunt Mode

Attach one of the two wires coming from the Neutral side of the current shunt to J3. This J3 connection is typically JP17, pin 2 on the Demo Board schematic. L2 and C3 minimize EMI noise entering through this connection.

Sensor Wiring

The following precautions apply to the sensor wiring:

1. Sensor wires may be shielded. Shielded wires are recommended for use with current shunts due to their low level signals. Use twisted pair wiring for internal wiring harnesses with or without shielding (STP or UTP).
2. When available, connect the cable shields to the board GND.
3. If cable shielding is not used, use unshielded twisted pair wire (UTP).
4. Keep sensor wires as short as possible.
5. It is possible to use ferrite clamps on sensor wiring to reduce common-mode noise.

Emulator Interface

Emulator Enable Pin (ICE_E)

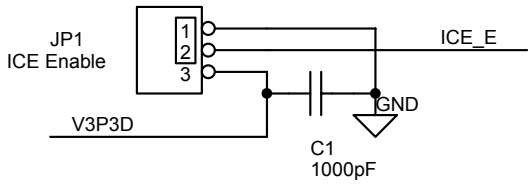

Figure 5: ICE_E Circuit

The ICE_E pin of the 71M652X can be sensitive to RF noise for long signal traces connecting the jumper pins to the ICE_E pin. Locate components JP1 and C1 adjacent to the device pin.

Emulator Signals

Since the emulator signals are also used as LCD segment outputs, they are best terminated with one 22pF capacitor per pin, as shown in Figure 6.

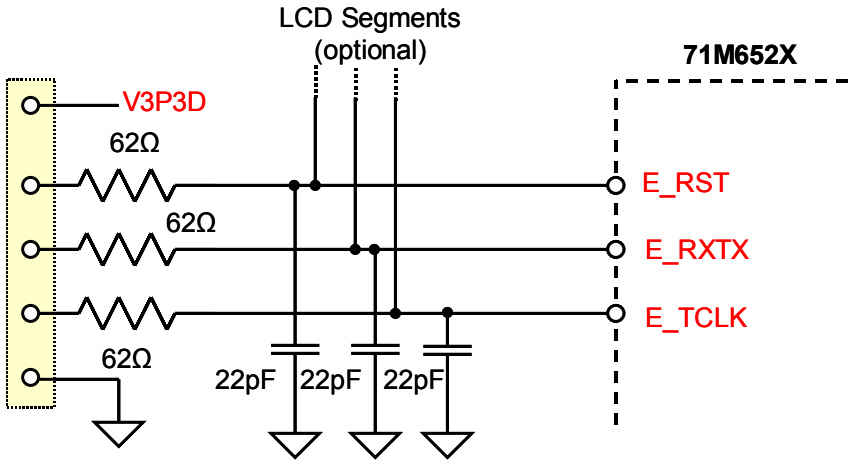

Figure 6: Termination of Emulator Signals

Other Circuit Elements

Power Supply Circuit

Figure 7 shows the recommended circuit for the standard capacitive power supply, as used on most 6521 Demo Boards. In general, transformer-based power supplies will provide better EMC/EMI test results.

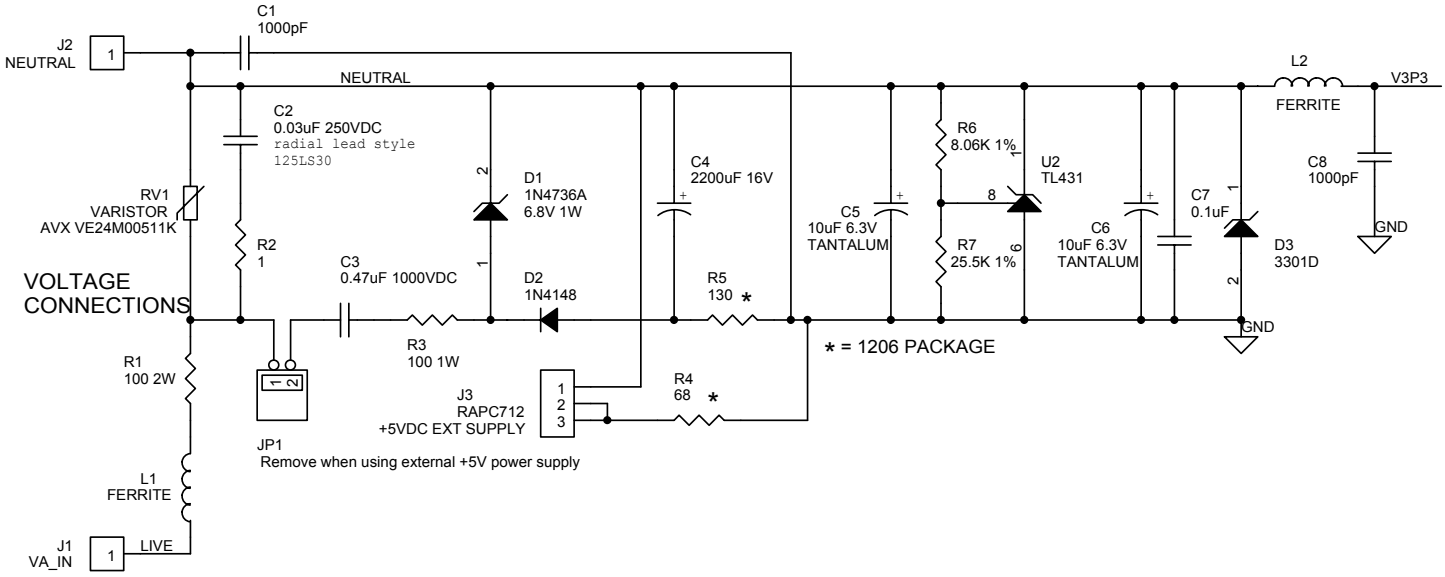

Figure 7: Power Supply Circuit

Key precautions recommended for the power supply circuit are:

1. The ferrite bead L2 at the V3P3 output minimizes high-frequency EMI noise.
2. A TVS (Transient Voltage Suppressor, D3) is added to clamp the V3P3 supply voltage to 3.3V. This device may be a bi-directional clamping device to prevent high voltage peaks from entering the circuit, e.g. the SEMTECH UCLAMP3301D.
3. The resistor R1 is added in series to the varistor (MOV) to limit the surge current. This resistor will cause a voltage drop that helps to protect both the varistor and the meter circuitry. Use a flame-proof type 100Ω resistor rated 2W to 5W.
4. The high-voltage capacitor C2 is added in parallel to the varistor to suppress high-frequency EMI noise. The series resistor R2 (1Ω) dampens oscillations that may occur due to the effective impedance of the power supply.
5. C7 and C8 suppress high-frequency EMI noise.
6. Improved EFT immunity is achieved by replacing C5 and C6 with ceramic type capacitors of values between 10uF to 47uF (even though the Demo Board utilizes Tantalum).

Reset Circuit

The 71M652X does not require an external reset circuit for normal operation. The device incorporates internal power monitoring capability and connecting the RESET pin to ground eliminates device resets due to EFT events. The following circuit is only recommended for program development purposes facilitating manual program restarts. Based on the placement of R2 one can use the around 10k to 100Ohms. C1 is optional.

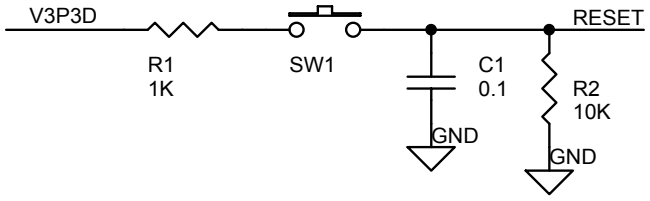

Figure 8: Reset Circuit

The RESET pin of the 71M652X can be extremely sensitive to RF noise for Long signal traces while connecting the discrete components to the reset pin. Locate components C1 and R2 adjacent to the device pin. Alternatively, the above reset circuitry can be located on the printed circuit board and R2 populated with a close to zero ohm resistor for production purposes.

PB (Push-Button) Circuit

The PB pin is programmed to provide an alternate display function. Its push button circuitry is identical the reset circuit shown above. The same precautions apply to the PB circuit. If the PB function is not required, connect the PB pin to ground.

V1 Circuit

The V1 input pin detects power faults and provides a means to disable the hardware watchdog timer for debugging purposes. When the voltage at the V1 pin falls below +1.6V the device enters its power down mode. When the voltage at the V1 pin is V3P3 (install jumper at TP1) the internal hardware watchdog timer is disabled.

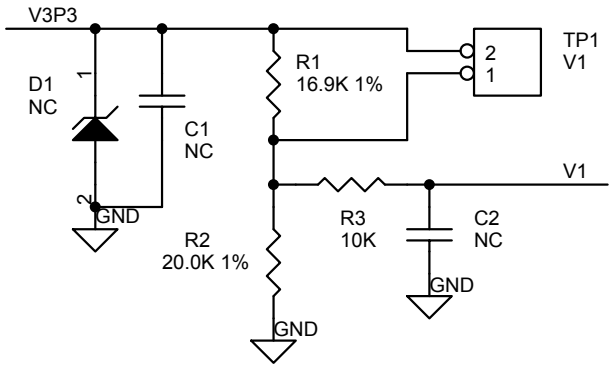

Figure 9: V1 Circuit

NC - No connect.

The V1 pin of the 71M652X is extremely sensitive to RF noise. Long signal traces connecting the various components to the V1 pin are not tolerated. Locate components R3 and C2 adjacent to the device pin. C2 is shown as not installed but is recommended as a provisional noise filter. Usage of additional components is dependent on the printed circuit board routing of the V3P3 signal.

The R1 and R2 component values are selected to provide a prompt response to a loss of line power. C4 (2200uF) shown in power supply circuit, provides sufficient holding power to allow the 71M652X to transition to battery power, if available.

Connecting Other IC Pins

All signals to and from the 71M652X IC must be examined carefully for EMC/EMI susceptibility. Proper signal termination minimizes unwanted resets, false readings and excessive radiated noise caused by RF fields.

The following list of precautions detail design considerations implemented for the other IC pins on the 71M6521X Demo Board:

1. Terminate all unused current and voltage inputs (**IA, IB, VA, VB**) to V3P3.
2. A 10µF tantalum capacitor must decouple the power and ground star points. The **V3P3A** pin and ground pin of the IC must have a clean and direct connection to the star points.
3. The V3P3SYS, V3P3A should be fed from the Stat point as described.
4. The GNDD and GNDA should also be fed from the GND stat point.
5. The **VREF** pin is to be unconnected. The Demo Board includes a test point only for debugging purposes.
6. Place a 0.1µF capacitor adjacent to the **V2P5** pin and ground.
7. No necessity to use external pull-up resistors for the emulator signals (**E_RST, E_TCLK, E_TXRX**). When ICE_E is ZERO these pins are configured as LCD segments and if unused can be terminated with 22pF.
8. E_RST need not have Capacitor of 1000pF,
9. CKTEST/SEG19 can be terminated with 22pF if unused as the clock signal for external circuitry.
10. Configure pins **OPT_TX** , **OPT_RX, TX and RX** as outputs when not used. If enabled, terminate **OPT_RX** with a 10K pull-down resistor and 100pF capacitor.
11. Place the crystal and its load capacitors adjacent to the device pins. Locating these components on the bottom side of the board minimizes trace length and minimizes interference from adjacent device signals.
12. Connect the **VBAT** pin to V3P3 when no battery is used.
13. Connect the **X4MHZ** and **TEST** pins directly to ground.

Layout Precautions

1. Four-layer printed circuit board structures provide the optimum performance with fastest time to market. The two internal layers are partitioned for ground and V3P3/V3P3D.
2. A two-layer board structure demands careful attention to the ground and V3P3A/3P3D signal integrity. Excessive copper voids and copper discontinuities will cause signal interference resulting in poor measurement accuracy and poor EFT/EMC performance.
   - Allocate the bottom layer for ground to maximize the ground surface under the device.
   - Use the top layer for signal routing.
   - Figure 10 and Figure 11 provide examples of a two-layer printed circuit board.
3. Physically separate the high-voltage and low-voltage sections of the board. In case of necessity use PCB cutouts to eliminate stray currents and arching.
4. Widen ground and V3P3 traces (using copper pour techniques) to create virtual planes. Use multiple free vias to “stitch” together top layer ground copper fills to the bottom layer ground plane structure.
5. Create a wide V3P3A plane structure to provide a stable reference for the measurement signals. Meter measurement performance is improved with wider V3P3A copper structures. Utilize a star point connection structure (“Kelvin” junction) on the top layer placed close to the V3P3A pin of the IC to bring together all V3P3 circuits.
6. Utilize a ground star point on the bottom side of the board for connecting the power supply, voltage and current input circuits. Place one of the 10uF capacitors across the ground and V3P3 star points.
7. The crystal and its load capacitors are positioned adjacent to the 71M652X IC. Placing the crystal and its load capacitors on the bottom side of the board results in the shortest trace lengths, isolation from adjacent device signals and protection from stray currents via the surrounding ground structure.
8. Whether a direct connection or terminated through a resistor or capacitor, the ground connections for the digital input signals RESET, PB, X4MHZ, ICE_E and TEST tie directly to the bottom layer ground structure.
9. Unrelated to EMI, the 68 pin version of the 71M6521 incorporates an exposed ground pad on the bottom side of the device. Do not route traces or place vias under the device.

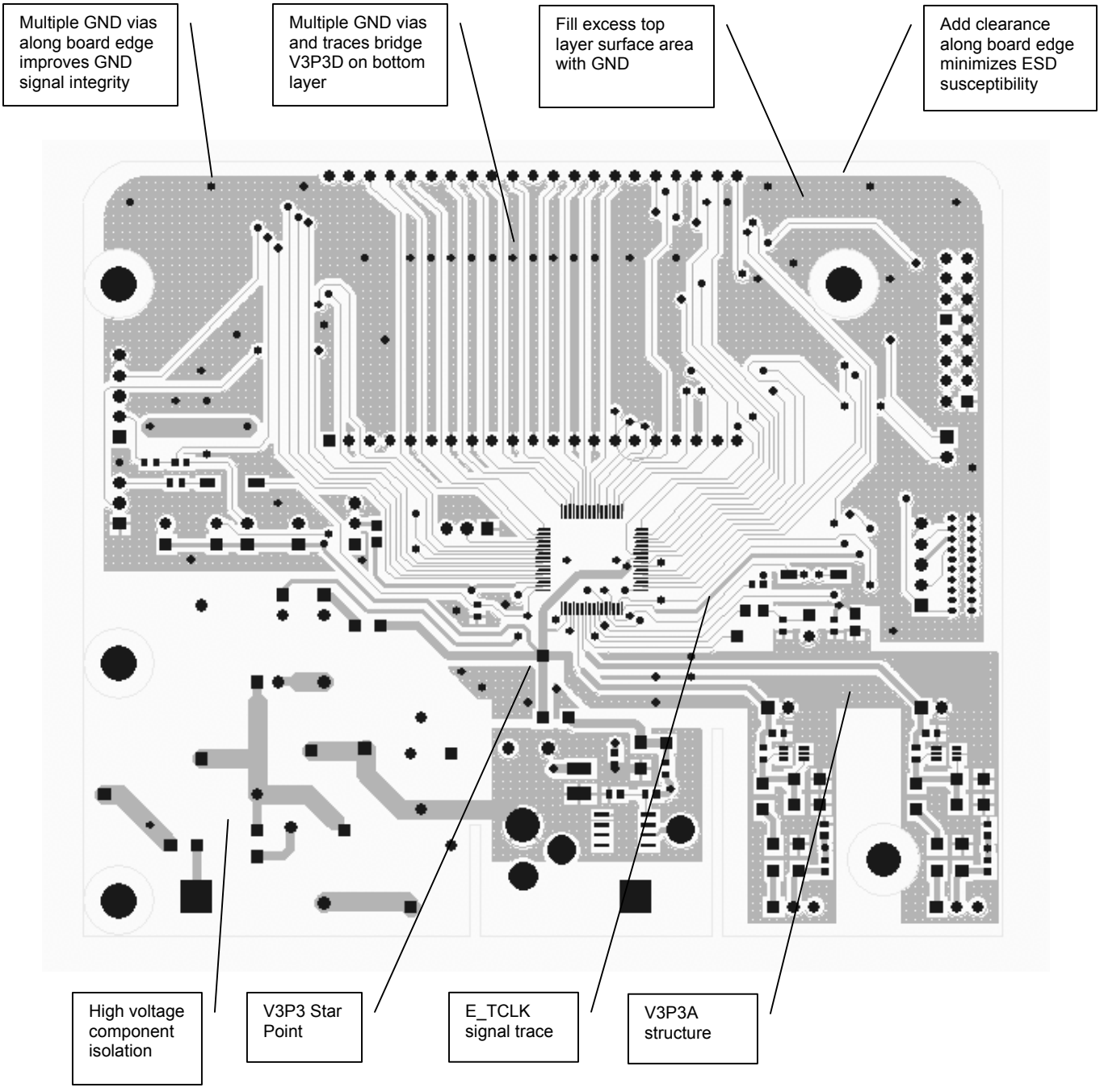

Figure 10: Top Copper Layer

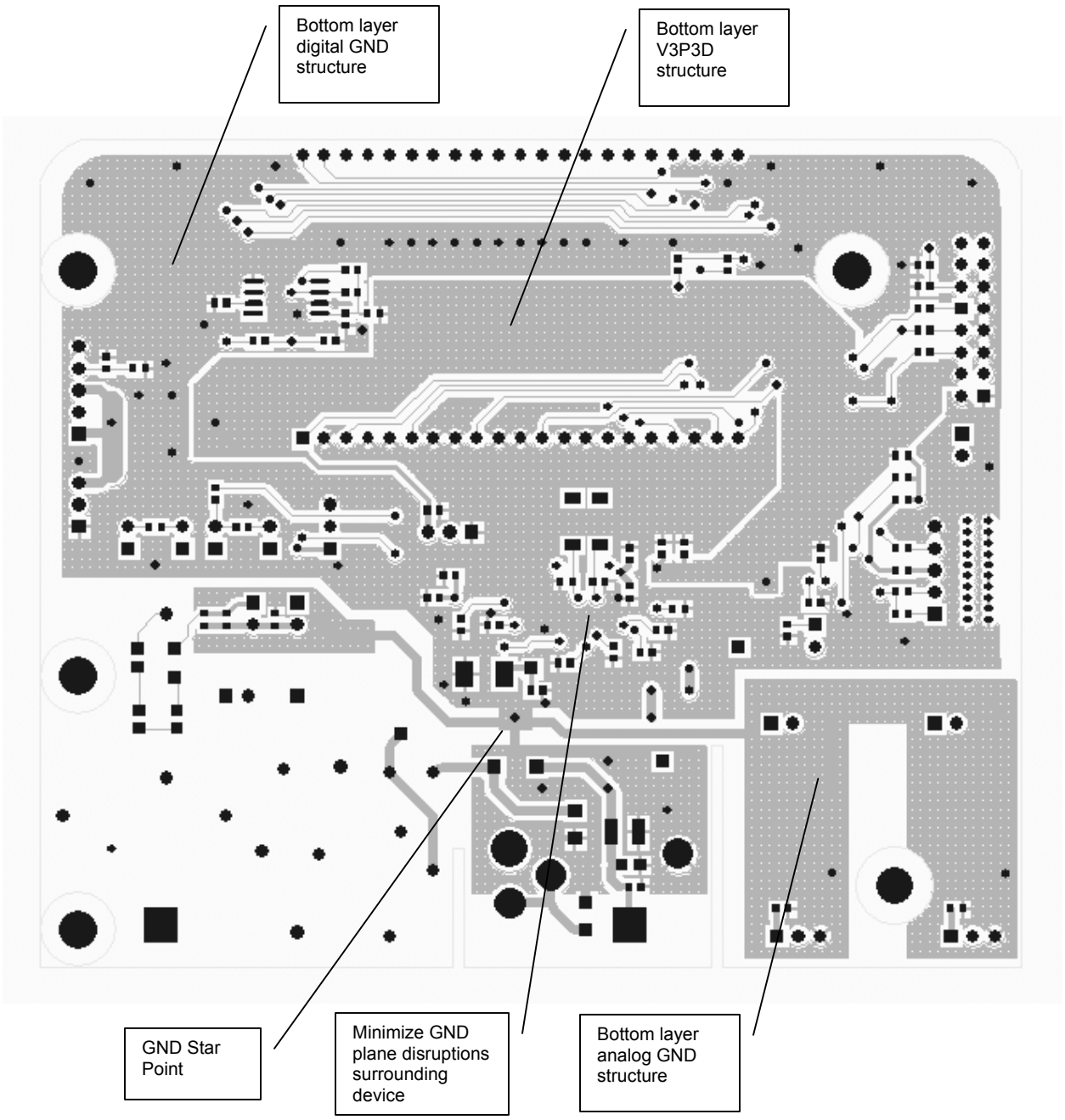

Figure 11: Bottom Copper Layer

Firmware Configuration Recommendations

1. Configure all unused DIO pins as outputs. This prevents unwanted signals from entering the IC.
2. Disable the emulator clock (configure *ECK_DIS* to 1) so that no 5MHz clock signal (I/O RAM 2005 Register Bit 5) is generated at the emulator port. This eliminates 5MHz clock signal emissions and ensures that the emulator port is disabled.
3. Disable the CKTEST clock output (by configuring *CKOUT_DIS* to 1) if not in use.
4. Place dummy interrupt service routines containing a RETI instruction at all locations pointed to by unused interrupt vectors.
5. All interrupt service routines (ISRs) are to be as short as possible and must minimize any memory manipulation operations.

External Components

After all careful circuit board layout design considerations have been incorporated and component selection optimization has been utilized, EMC/EMI testing may still fail to produce the desired results. The addition of external ferrite components to the sensor and power wires may be required.

The current shunt configuration is the most difficult application due to the direct connection of the NEUTRAL wire to the board's V3P3. External clamp-on ferrites or external toroid ferrites on the following wires provide additional noise suppression:

1. NEUTRAL power entry wire
2. Second NEUTRAL power entry wire
3. Current shunt sensor wires

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