AN_65XX_062

APPLICATION NOTE

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Methods for Power Conservation

Theory

The general idea of power conservation is to reduce the supply current, whereas the supply voltage has to be in the recommended range and cannot be varied by much without affecting the IC performance. The supply current can be reduced by disabling unneeded circuit parts, reducing the clock frequency of active parts, and by eliminating leakage.

Advantages

Saving power in the meter internals multiplies the efficiency. A direct effect, besides improving the supply current specification, is the reduction in component size used for the power supply. In some cases, reducing the power consumption may enable a competitive advantage by permitting a high precision TSC meter IC to replace a lower-precision general-purpose IC that uses less current.

Various Methods for Power Conservation

Using Optimized MPU Code

Version 3 and earlier versions of the Demo Codes for the 71M6511 and 71M6513 were not optimized for speed, and even at the full 4.9 MHz MPU clock speed, they used almost 400 ms of each 999 ms accumulation interval for calculations. In particular, they used a slow, proprietary multiple-precision arithmetic package.

Version 4 and later versions of the Demo Codes perform the equivalent calculations in 50 ms or less. They include the following improvements:

1. Wh are integrated by adding the CE's *WnSUM* registers to a 32 bit count. When this exceeds 1 Wh, 1 Wh of counts is subtracted, and 1 is added to a separate 32-bit count of Wh. The count of Wh can be divided by 1000 to display energy in kWh. When the count of Wh reaches 10^9 it turns over to zero. This system has no round-off error. VARh and VAh accumulations for demand, as well as export data are calculated in the same way.

2. Other values, like V, A, and VA are calculated only when they are to be displayed.

3. Calculations like V, A, etc. use the floating point algorithms of the C compiler. The floating point library has 24 bits of precision and is more accurate than most measurements for a one-second accumulation interval. The Keil C compiler's floating point is also standardized (to IEEE 754), validated, convenient, and extremely optimized.

4. The MPU's PDATA memory space window is set to cover the area that contains the CE data, and the CE variables are defined in the MPU code as PDATA types. So, the MPU reads the CE data with fast PDATA instructions that can use any available register as an index. Historic 8051 MPUs could address 256 bytes of external memory by setting a port, and then using the instruction MOVX A,@Ri and MOVX @Ri,A. In TSC's 80510 MPUs, the "port" is SFR 0xBF, ADRMSB. It is usually set in the startup assembly code. In the 71M651X and 71M652X, ADRMSB is set to 0x07, because the copy of the CE's data is at 0x0700. In the 71M653X and 71M654X, there is no need to copy the data, so ADRMSB is set to 0x02 because the start of the CE data is 0x0200.
5. If the MPU copies the CE data, as in the 71M651X and 71M652X, using PDATA addresses for the destination is at least 4x faster than code using a single DPTR as the index register. Some customers

have achieved good results by writing the copy operation in assembly language and using the second DPTR, of the 85150 MPU, but this is theoretically not as fast as the PDATA copy because the register select bit must be changed twice per loop. The PDATA instructions can use any of 8 registers as the PDATA index register.

Reducing the MPU Clock Rate

In the meter SOCs, the MPU uses power proportionately to its clock rate. A slower clock rate is better for power consumption. Version 4+ MPU code can usually function with MPU clock rates as slow as 600 kHz with acceptable performance.

Using the *STOP* Bit

If the MPU code is efficient enough to have substantial idle time, this time can be used to reduce power.

In some meter codes (e.g. V4+ TSC Demo Code), more than 95% of the MPU's time can be spent waiting for events. If the MPU is waiting in a loop, it is wasting power by constantly fetching op-codes from the flash memory. All TSC meter SOCs with an 80510 MPU include a power control register, *PCON*, at SFR 0x87. Setting bit 1 (*STOP* bit) stops the MPU and inhibits flash accesses. Other bits in this register should not be changed. For example, bit 7 helps set the serial BAUD rate.

After the *STOP* bit is set, the MPU stops and wakes only at the next interrupt. When the interrupt occurs, the *STOP* bit in the PCON register is cleared automatically.

If the code to stop the MPU is located in the main loop, and events are started by interrupts (as in the TSC Demo Codes), the operation of the meter will appear unchanged, and save some power.

Not every interrupt should be able to wake and run the main loop. Sometimes the interrupt can handle everything without help from the main loop. A simple solution can save most of the power that would otherwise be wasted by running the main loop. For example:

```
volatile bool wake_request; // Set if an important interrupt needs the main loop.
…
main (void)
{
…
    while (true) // Do main loop
    {
        wd_reset() // reset the watchdog.
        while (!wake_request)          // Does an interrupt need the main loop?
        {
            PCON |= 2;  // Stop the MPU
        }
        wake_request = 0;
        …
    }
}
```

Then, when the interrupt needs the main loop to run:

```
    wake_request = 1;
```

Savings vary by code, MPU type and clock rate, but there are real savings. Some examples are shown in Table 1.

Table 1: Supply Current Comparison

IC	MPU Clock Speed	Supply Current, w/o *STOP* *)	Supply Current, with *STOP* *)
71M6511	4.9 MHz	11.5	10.4
71M6511	600 kHz	7.9	7.8
71M6521	4.9 MHz	10.4	9
71M6521	600 kHz	7.46	7.43
71M6533	4.9 MHz	14.5	12.9
71M6533	600 kHz	12.7	12.1

* **Measured on one Unit, given in [mA]**

During debugging with the emulator, the emulator is sometimes unable to synchronize to a stopped 80510 MPU. In that case, it detects this state and requests the operator to reset the MPU.

Optimizing CE Code

In the 71M652X and 71M653X series of metering ICs, shorter, simpler CE code can help to consume significantly less power. For example, on the 71M6521, disabling the CE can drop the typical power usage by 1.2 mA. This means that simpler CE code of 3/4 of the original the size should save 0.3 mA. In a high-volume application, using simplified custom CE code with fewer, i.e. only the required features, can be practical. For example, VARh and frequency measurements may be unnecessary for some applications.

A similar effect occurs in the 71M651X series, but the current saved is about one eighth of the current saved in the 71M652X and 71M653X series, which means that optimizing CE code is less valuable.

Optimizing LCD Control

The LCDs should be run at the slowest clock that is visually acceptable, with the minimum number of states, and with 5V boost disabled, if possible. The LCD DAC, if present, should be set to the minimum contrast in order to minimize the total drive current.

Miscellaneous Power Saving Methods

Clean PCBs also have less leakage off the VBAT and VBAT_RTC pins if the area around these pins is thoroughly cleaned and free of solder flux residue and other types of contamination. This technique, of course, applies to the current draw from the batteries, and the power savings are negligible in mission mode.

Also, reducing strobe times for internal memory can help to reduce power. Strobe-width settings are not available on all Teridian metering ICs, but on the 71M651X series, setting FLSH66X can save 0.16 mA at 4.9 MHz.

Output pins with low impedances and high frequencies should be turned off to save power. For example, the test multiplexer pin, TMUX (or TMUXOUT and TMUX2OUT on some ICs) should be set to a DC output like ground. The clock test outputs (CKTEST) should be disabled.

The emulator clock can be disabled as well. However, immediately disabling the emulator clock can prevent maintenance and factory rework. It is better to disable it at least several seconds after reset.

Finally, TSC meter SOCs can save about 5% of the power (as compared to nominal supply voltage) if they operate in the lower quarter of their voltage range, near 3.15 V. This requires tighter component tolerances for the board power supply, but these may be inexpensive compared to the value created by the change.

Revision History

Revision	Date	Description
Rev. 1.0	9/29/2009	First release

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